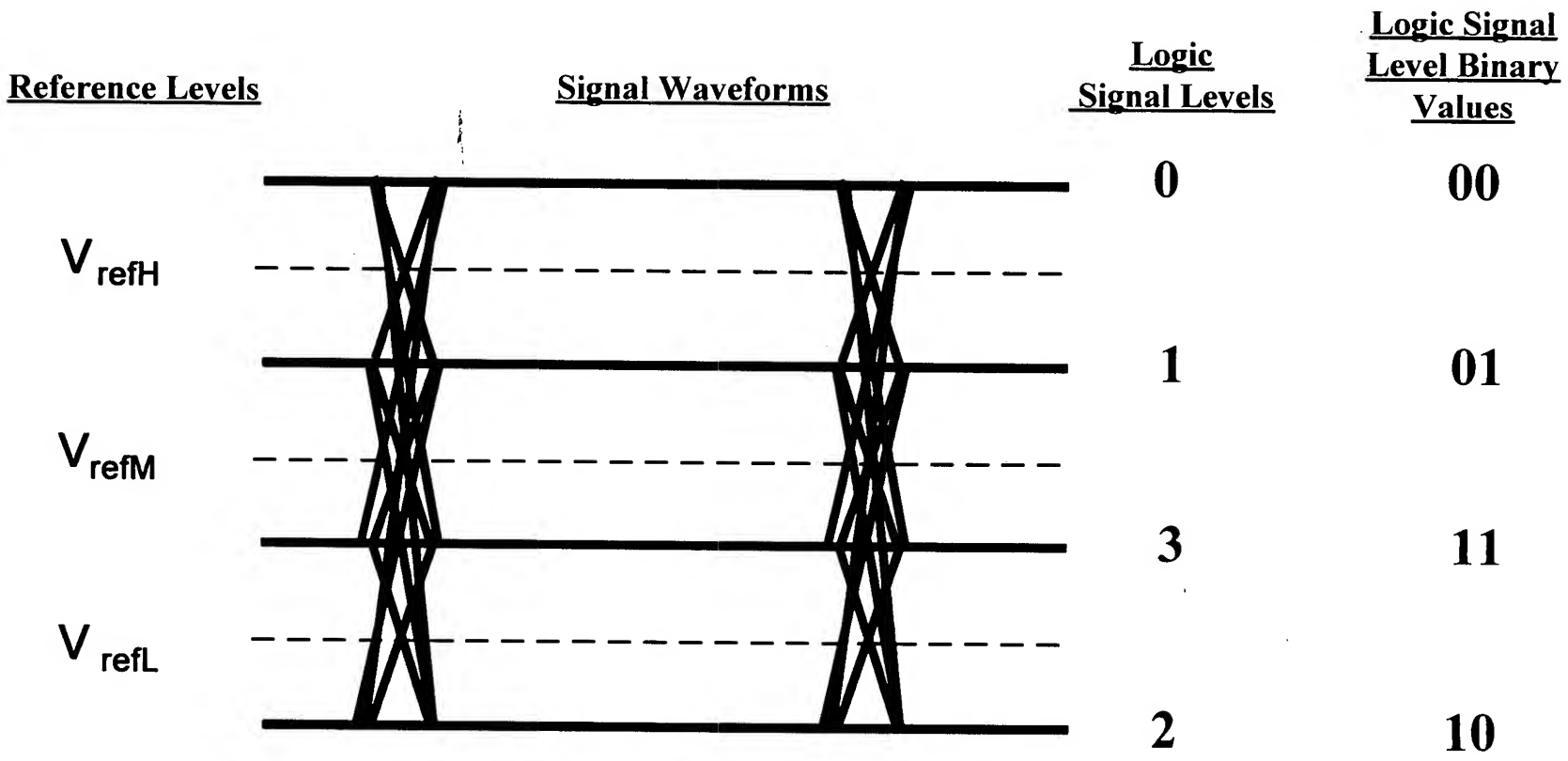
Reference Levels
Signal Waveforms
Logic Signal Levels
Logic Signal Level Binary Values
V refH
V refM
V refL
0
1
3
2
00
01
11
10

Figure 1

V_{in}	ia	ib
$V_{in} > V_{refH}$	i	2i
$V_{refH} > V_{in} > V_{refL}$	2i	i
$V_{in} < V_{refL}$	i	2i

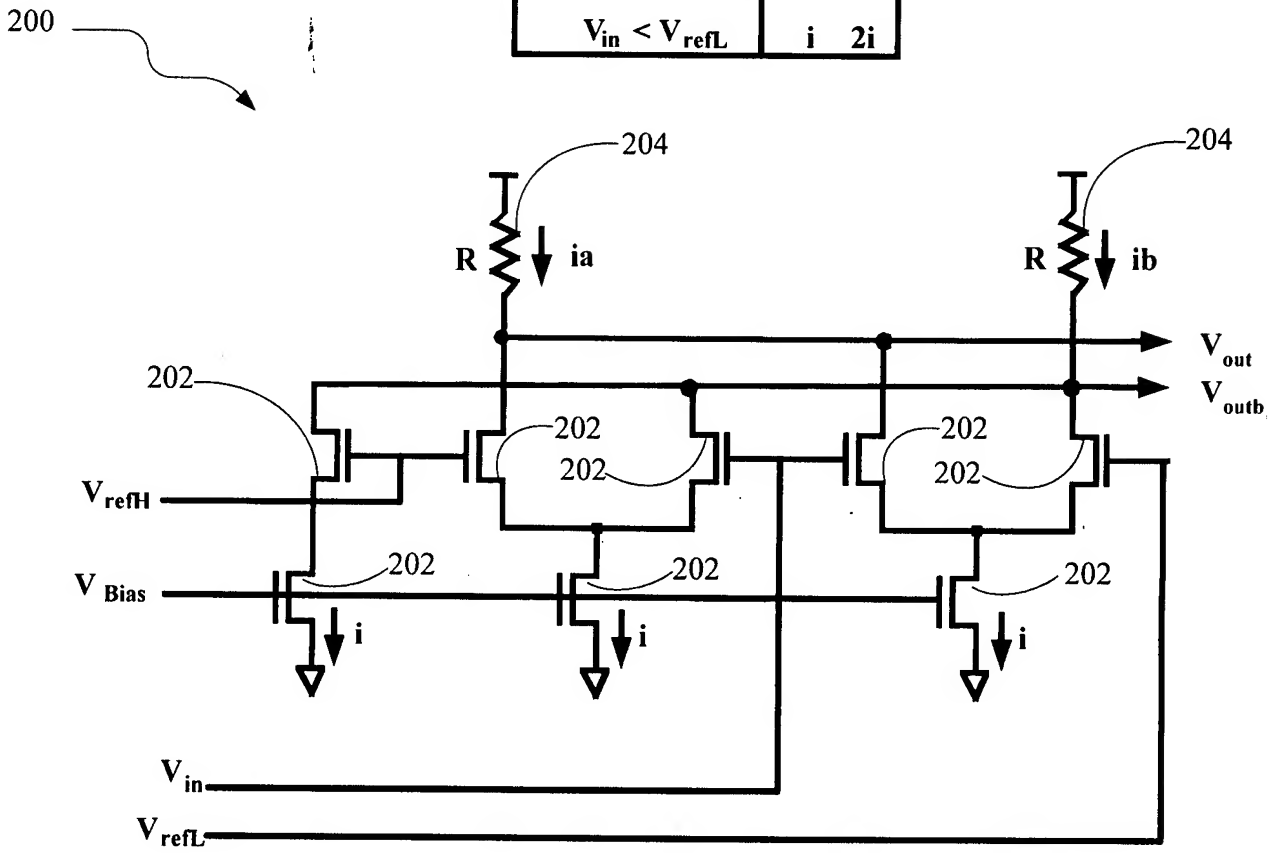

Figure 2

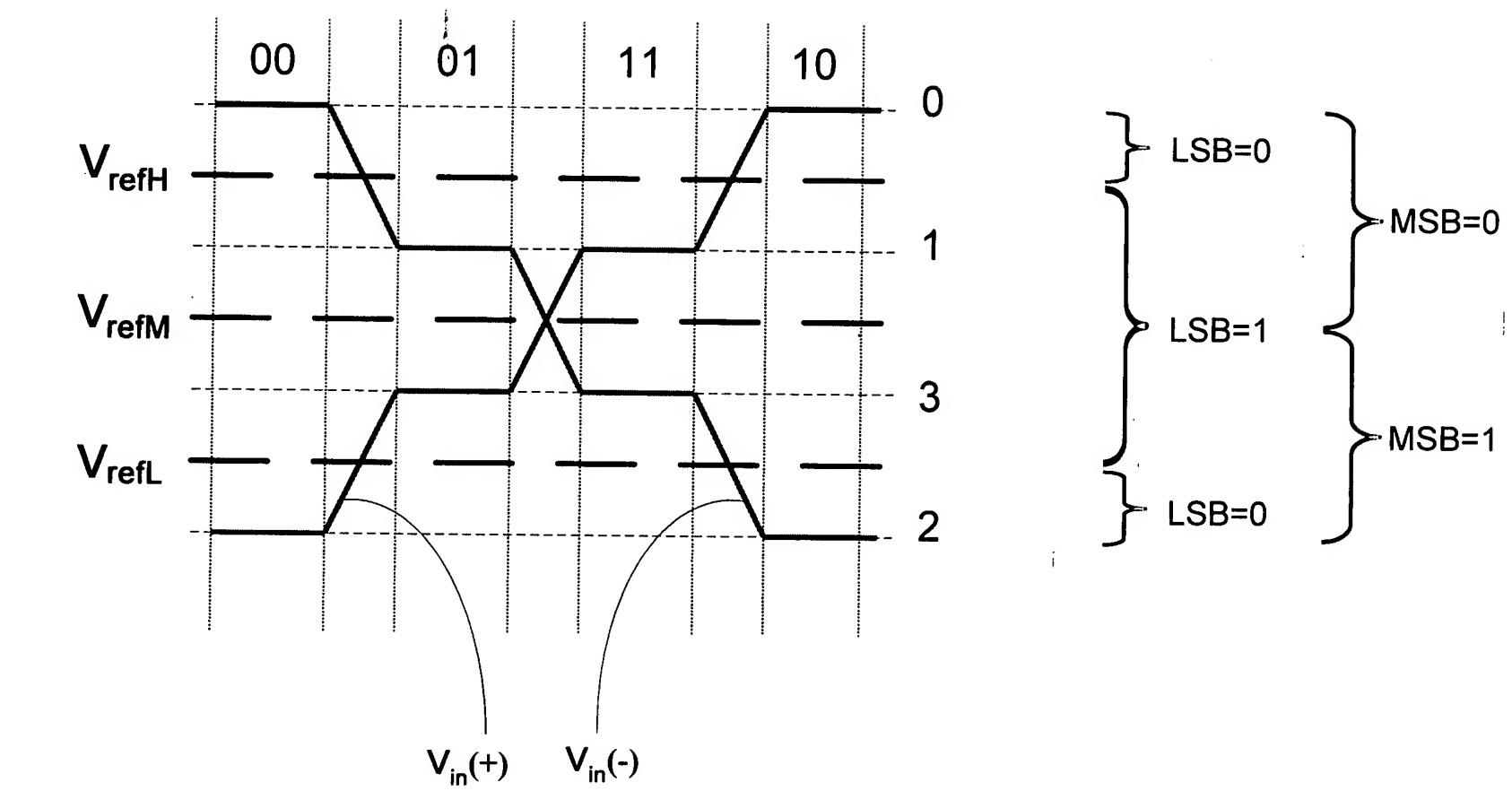
Reference Levels
Signal Waveforms and Differential Logic Signal Level Binary Values
V_{in}(-) Logic Signal Levels
V_{in}(-) MSB & LSB Value Ranges
00
01
11
10
0
1
3
2
V_{refH}
V_{refM}
V_{refL}
V_{in}(+)
V_{in}(-)
LSB=0
LSB=1
LSB=0
MSB=0
MSB=1

Figure 3

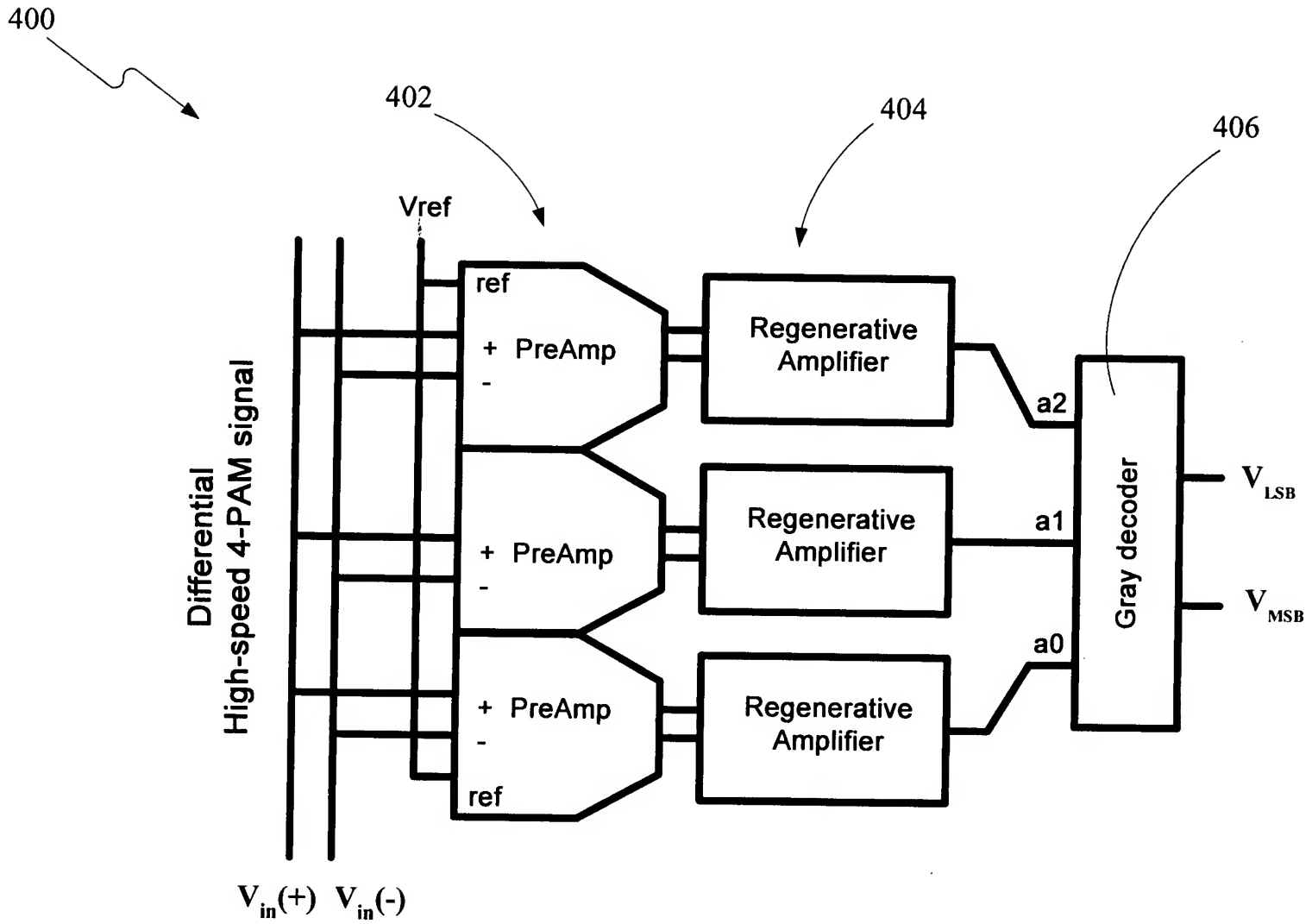
400
402
404
406
Vref
ref
+ PreAmp
-
+ PreAmp
-
+ PreAmp
-
ref
Regenerative Amplifier
Regenerative Amplifier
Regenerative Amplifier
a2
a1
a0
Gray decoder
V_{LSB}
V_{MSB}
Differential High-speed 4-PAM signal
$V_{in}(+)$ $V_{in}(-)$

Figure 4A

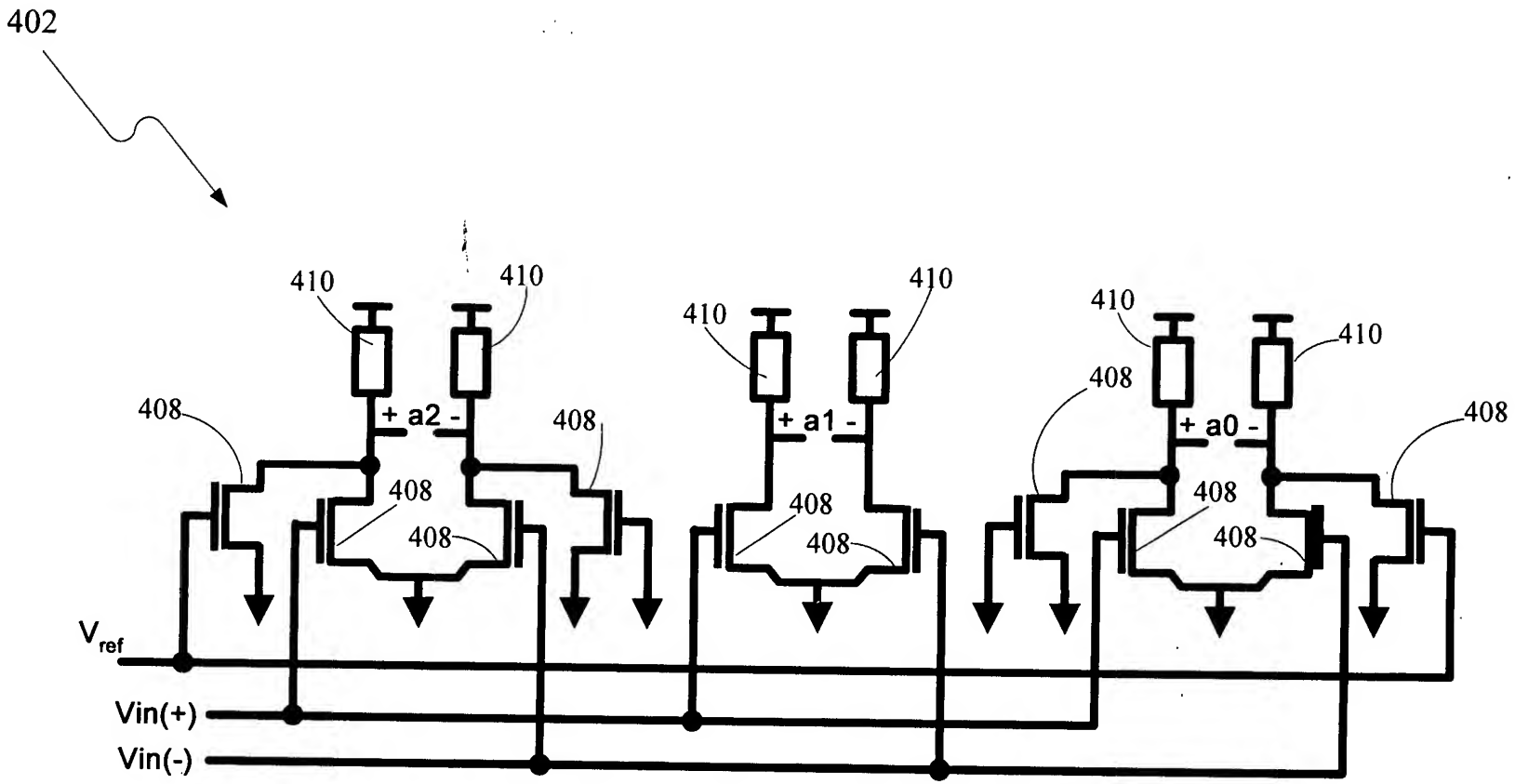
402
410
410
410
410
410
410
408
408
408
408
408
408
408
408
408
+ a2 -
+ a1 -
+ a0 -
V_{ref}
Vin(+)
Vin(-)

Figure 4B

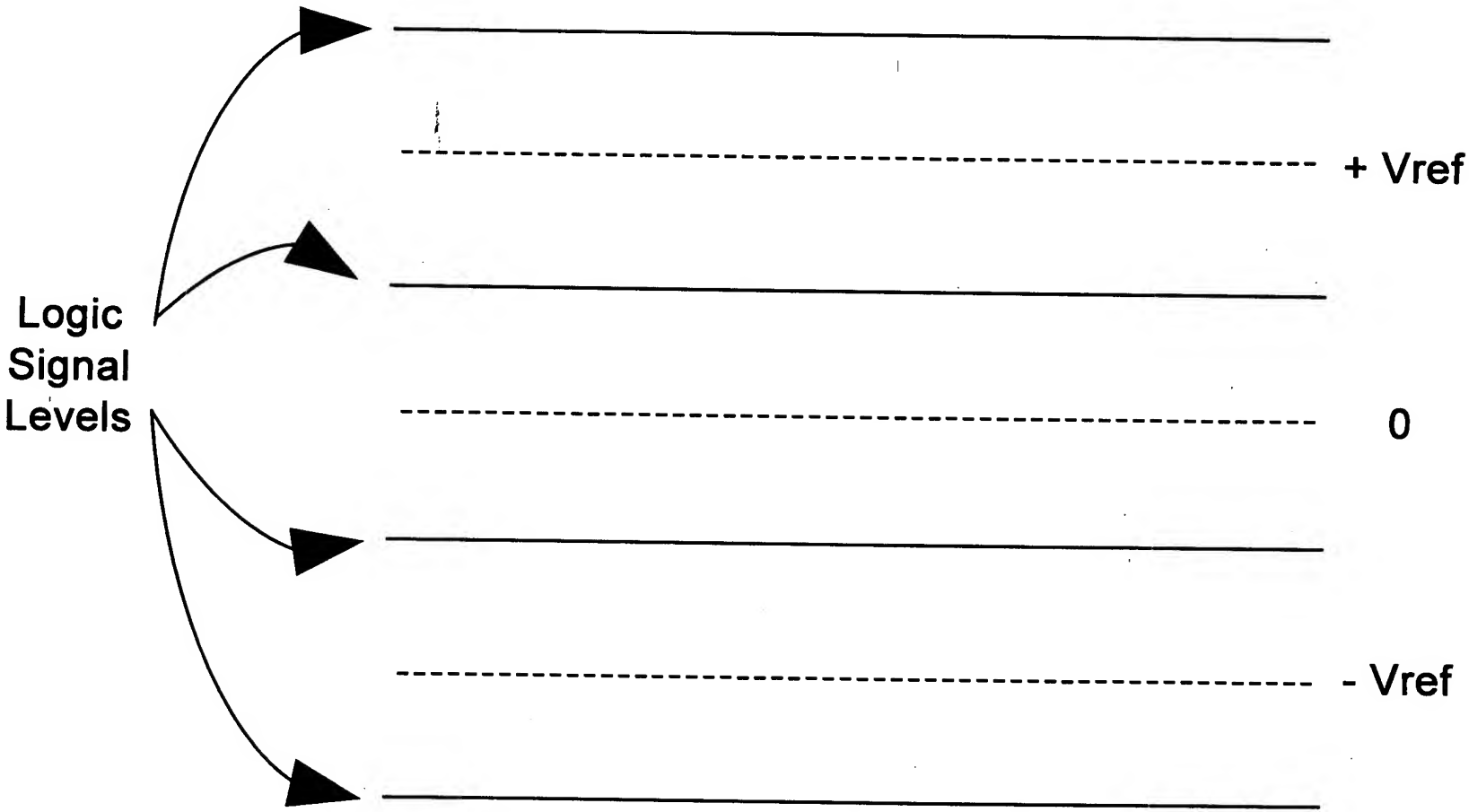

Figure 4C

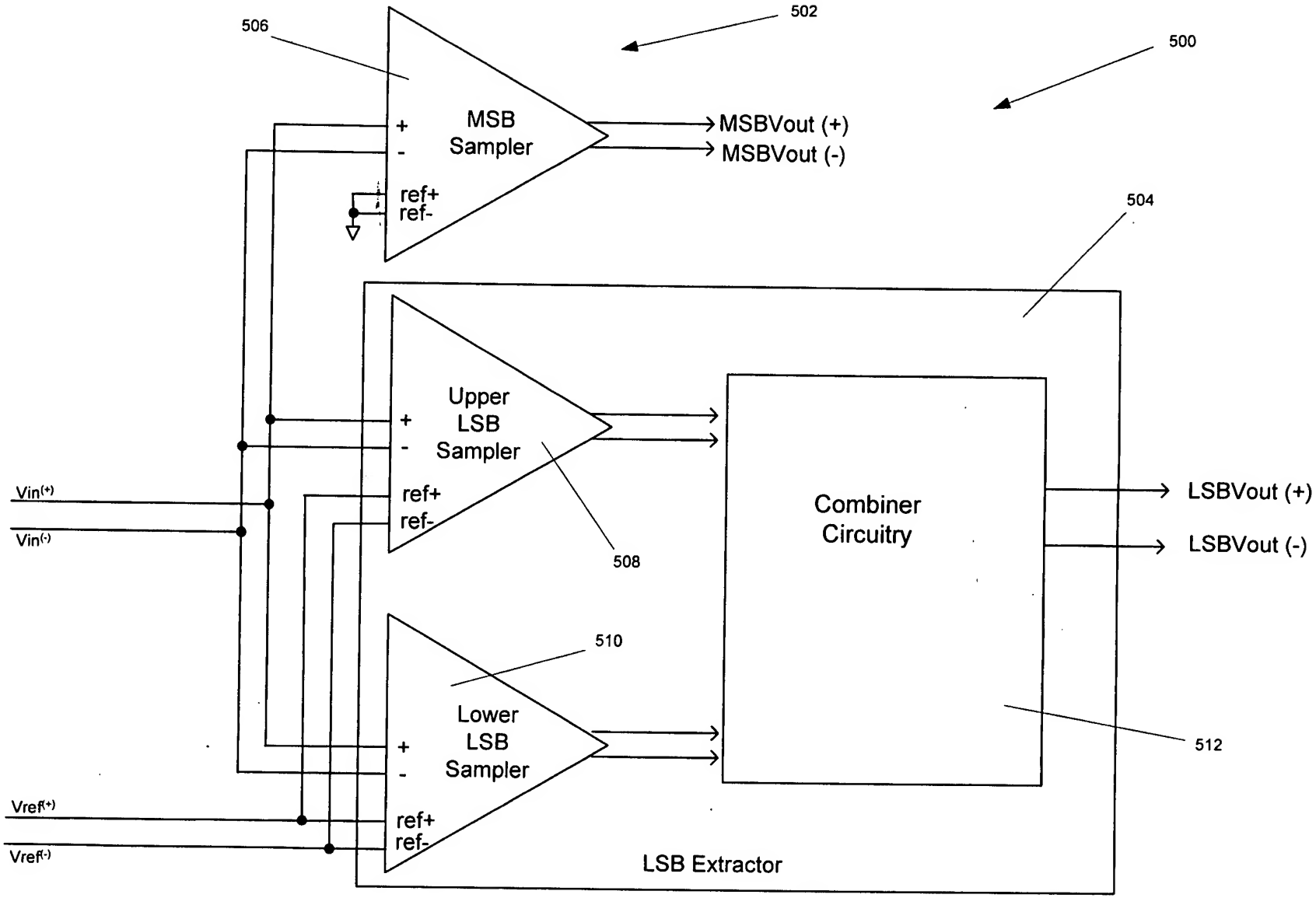
502
500
506
MSB
Sampler
+
-
ref+
ref-
MSBVout (+)
MSBVout (-)
504
Upper
LSB
Sampler
+
-
ref+
ref-
508
Combiner
Circuitry
LSBVout (+)
LSBVout (-)
Vin(+)
Vin(-)
510
Lower
LSB
Sampler
+
-
ref+
ref-
512
Vref(+)
Vref(-)
LSB Extractor

Figure 5A

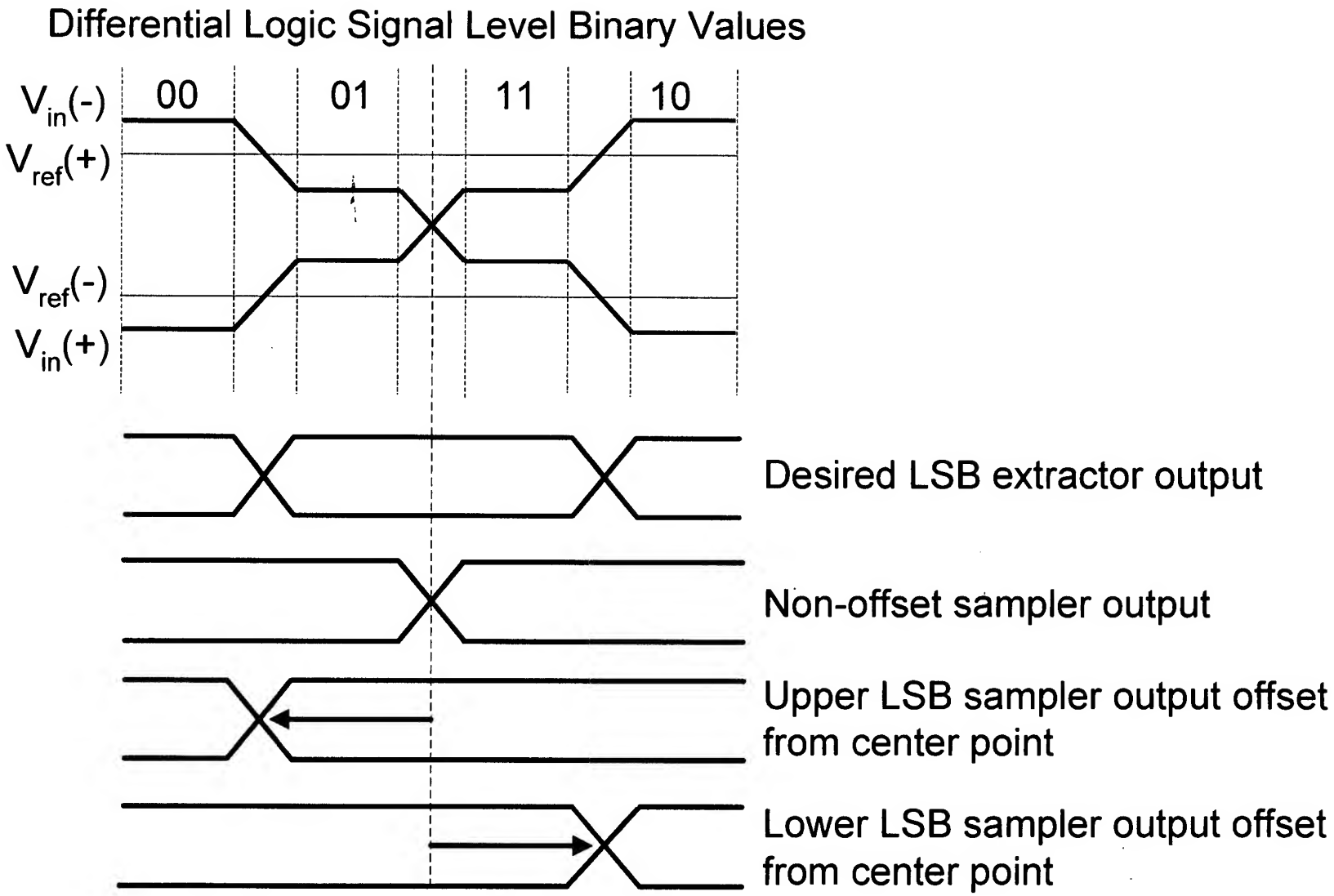
Differential Logic Signal Level Binary Values
V_{in}(-)
V_{ref}(+)
V_{ref}(-)
V_{in}(+)
00
01
11
10
Desired LSB extractor output
Non-offset sampler output
Upper LSB sampler output offset from center point
Lower LSB sampler output offset from center point

Figure 5B

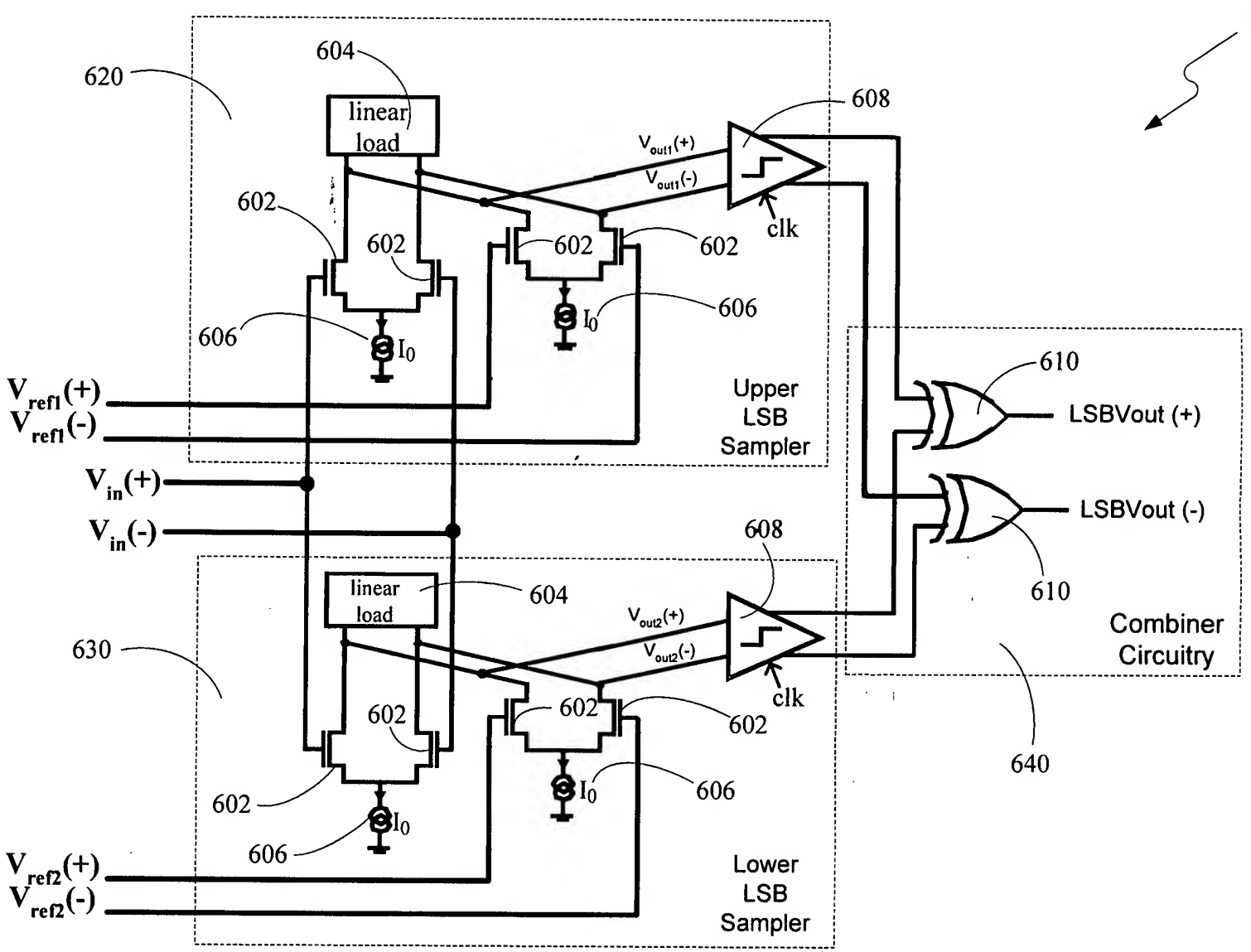
600
620
604
linear load
608
$V_{out1}(+)$
$V_{out1}(-)$
602
602
602
602
clk
606
606
I_0
I_0
$V_{ref1}(+)$
$V_{ref1}(-)$
Upper LSB Sampler
610
LSBVout (+)
$V_{in}(+)$
$V_{in}(-)$
LSBVout (-)
608
610
Combiner Circuitry
linear load
604
630
$V_{out2}(+)$
$V_{out2}(-)$
clk
602
602
602
602
640
606
606
I_0
I_0
$V_{ref2}(+)$
$V_{ref2}(-)$
Lower LSB Sampler

Figure 6

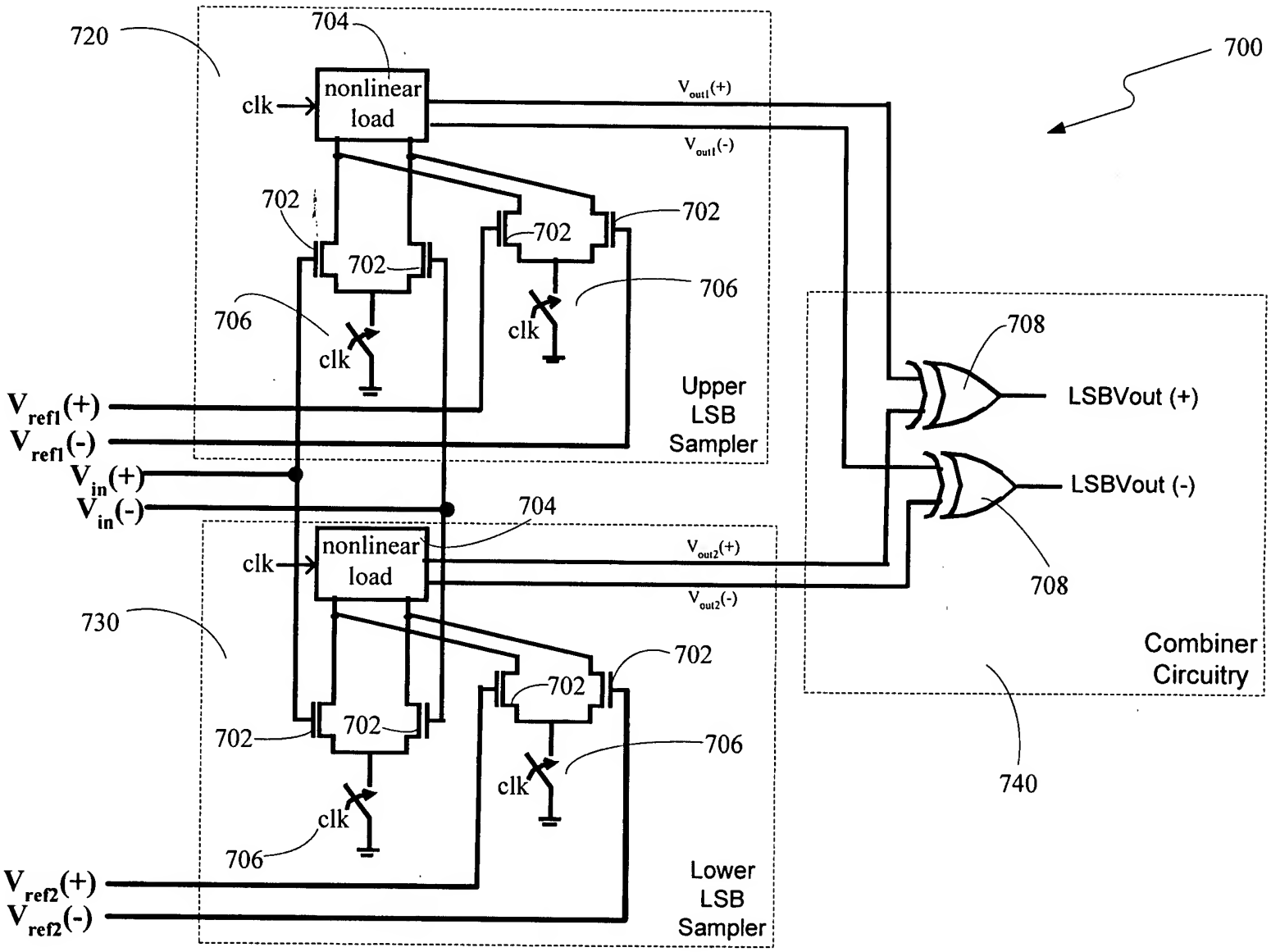
720
704
nonlinear load
clk
$V_{out1}(+)$
$V_{out1}(-)$
702
706
clk
Upper LSB Sampler
$V_{ref1}(+)$
$V_{ref1}(-)$
$V_{in}(+)$
$V_{in}(-)$
730
$V_{out2}(+)$
$V_{out2}(-)$
Lower LSB Sampler
$V_{ref2}(+)$
$V_{ref2}(-)$
700
708
LSBVout (+)
LSBVout (-)
Combiner Circuitry
740

Figure 7

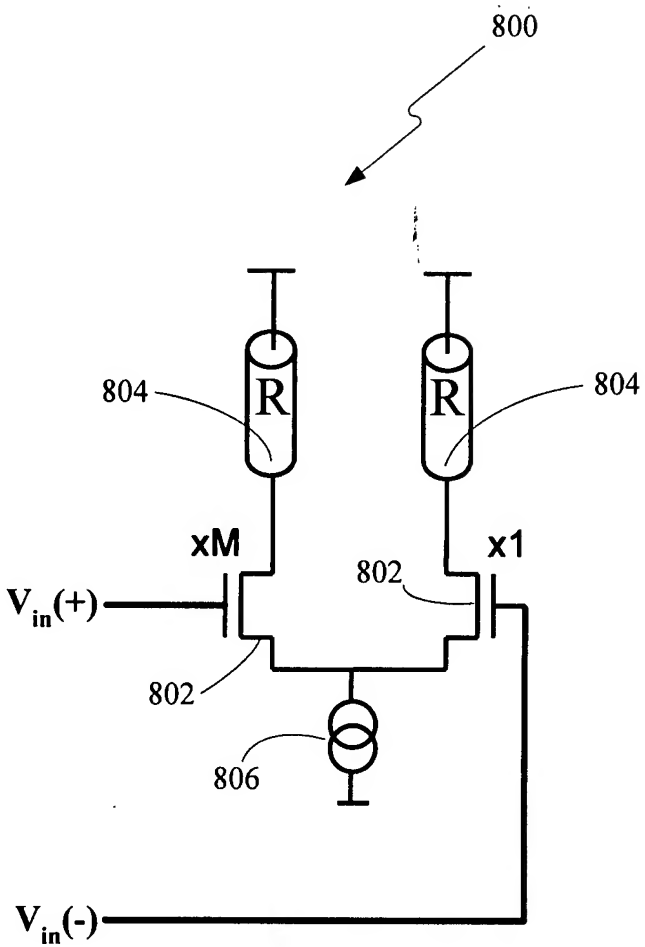

Figure 8A

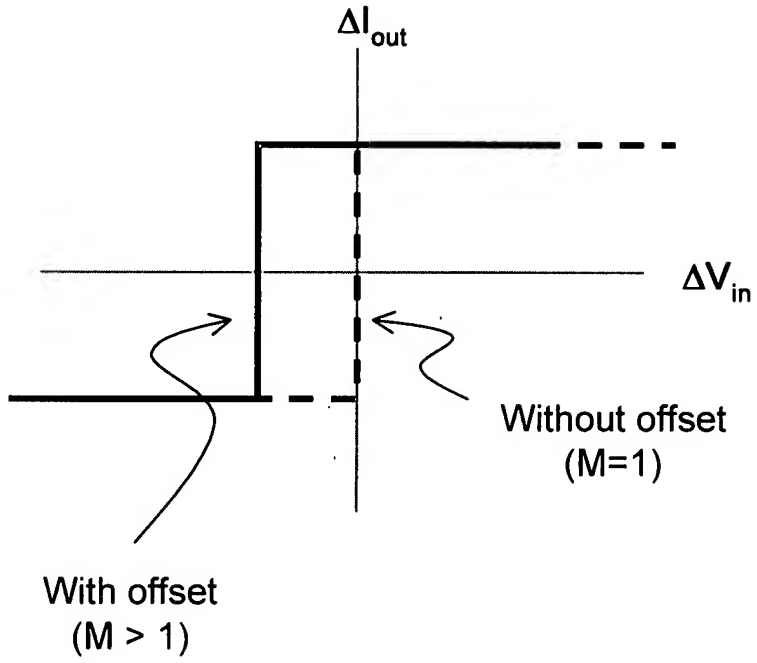

Figure 8B

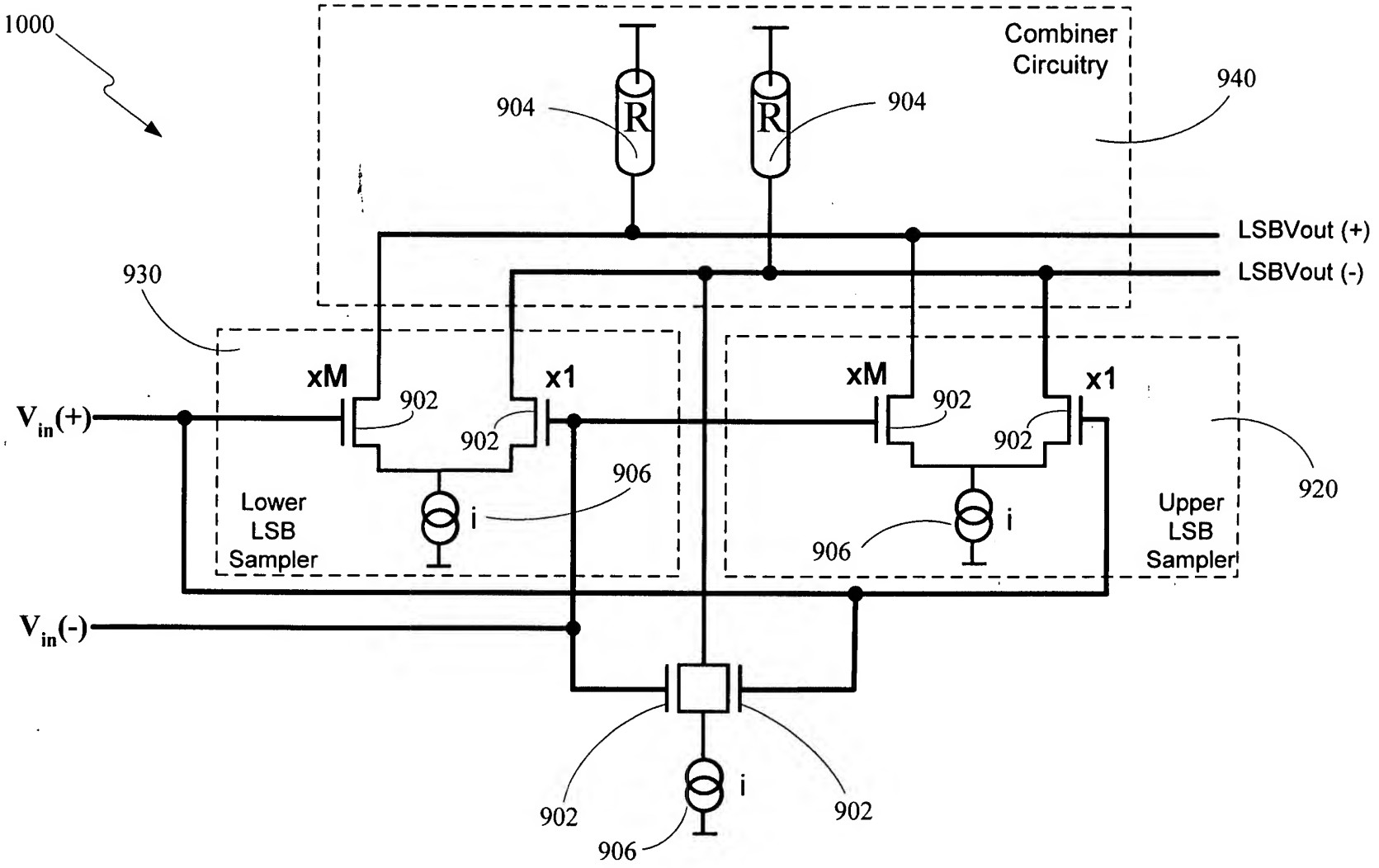
1000
Combiner Circuitry
940
904
R
R
904
LSBVout (+)
LSBVout (-)
930
xM
x1
902
902
906
Lower LSB Sampler
i
xM
x1
902
902
906
Upper LSB Sampler
920
i
V_{in}(+)
V_{in}(-)
902
902
906
i

Figure 9

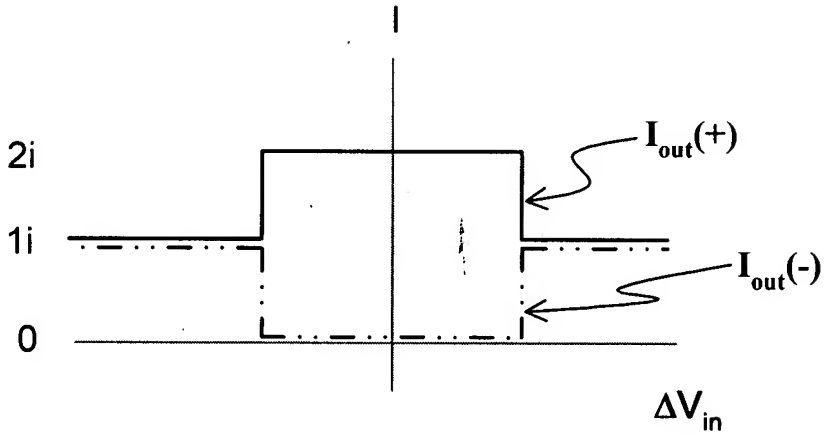

Figure 10A

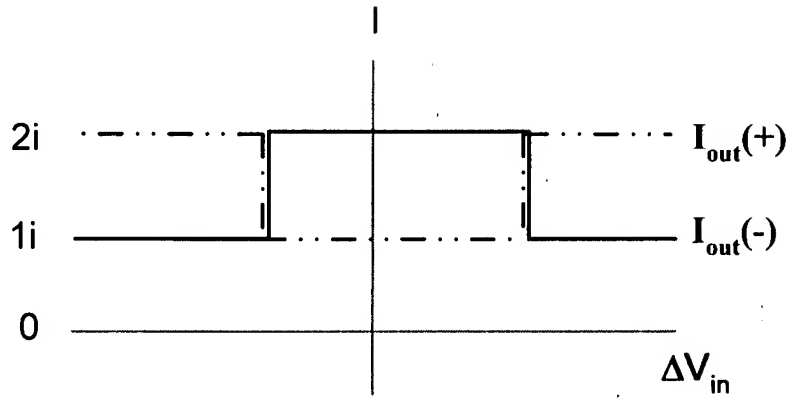

Figure 10B

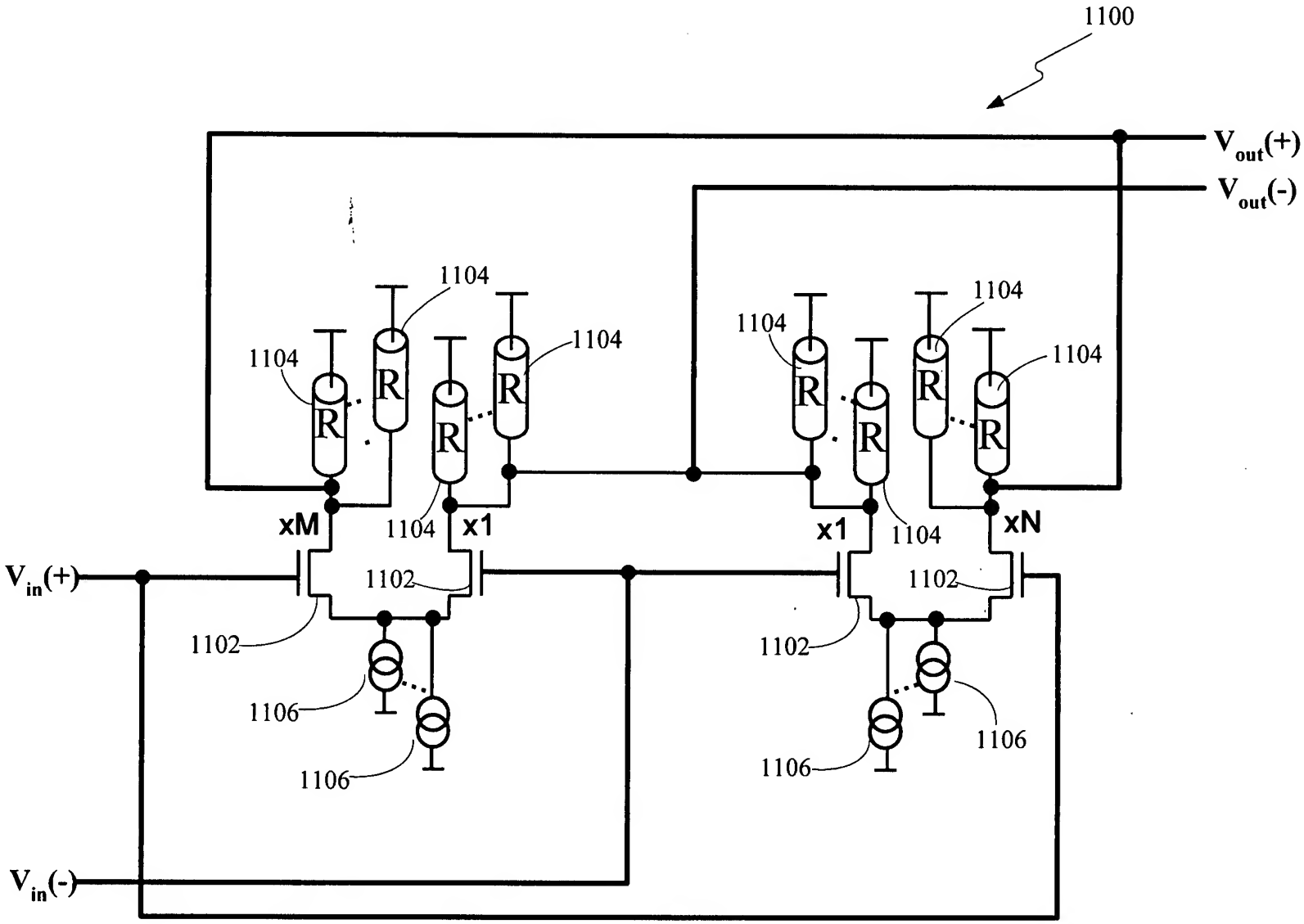

Figure 11

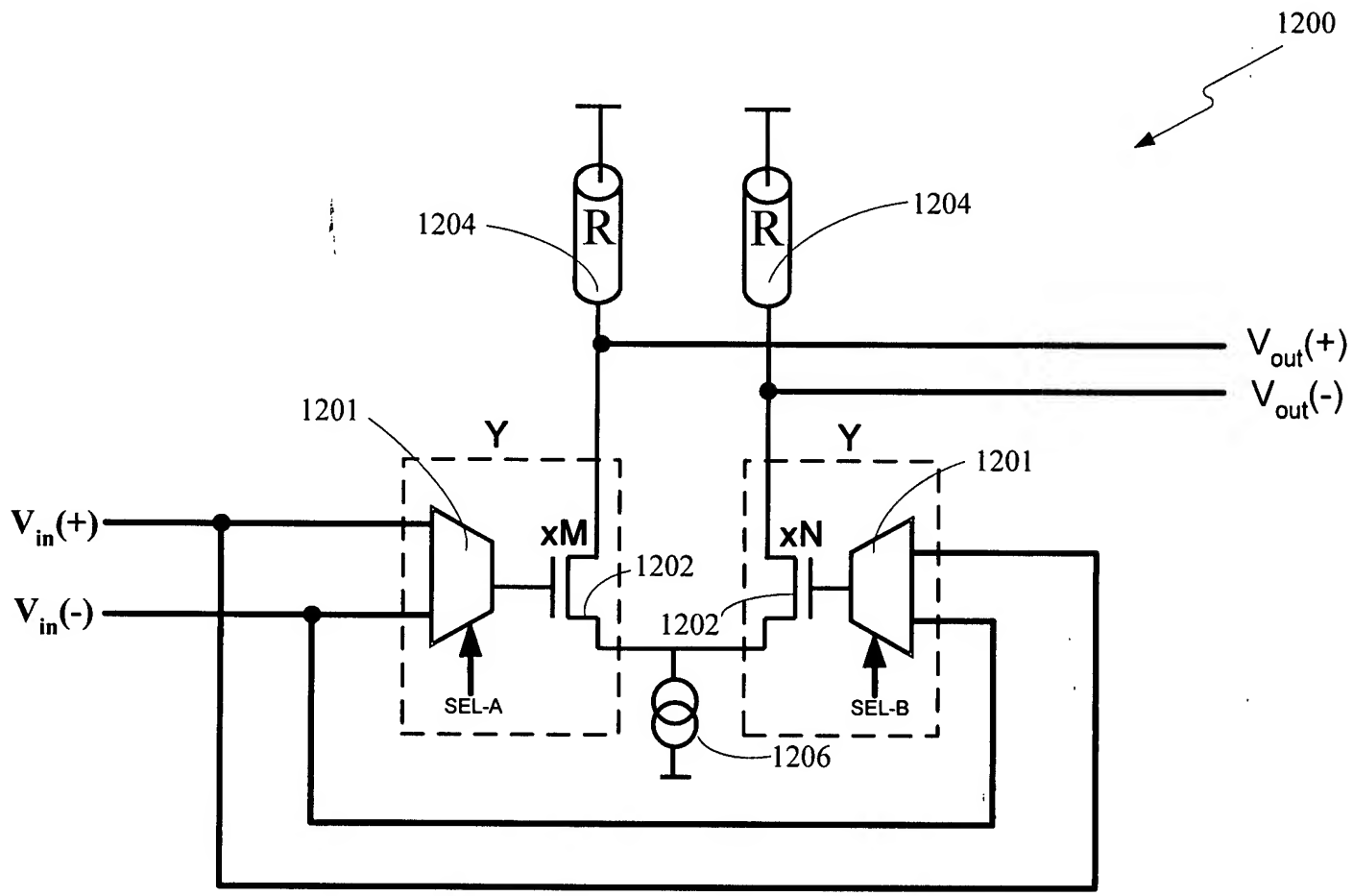
1200
1204
R
R
1204
$V_{out}(+)$
$V_{out}(-)$
1201
Y
Y
1201
$V_{in}(+)$
$V_{in}(-)$
xM
xN
1202
1202
SEL-A
SEL-B
1206

Figure 12

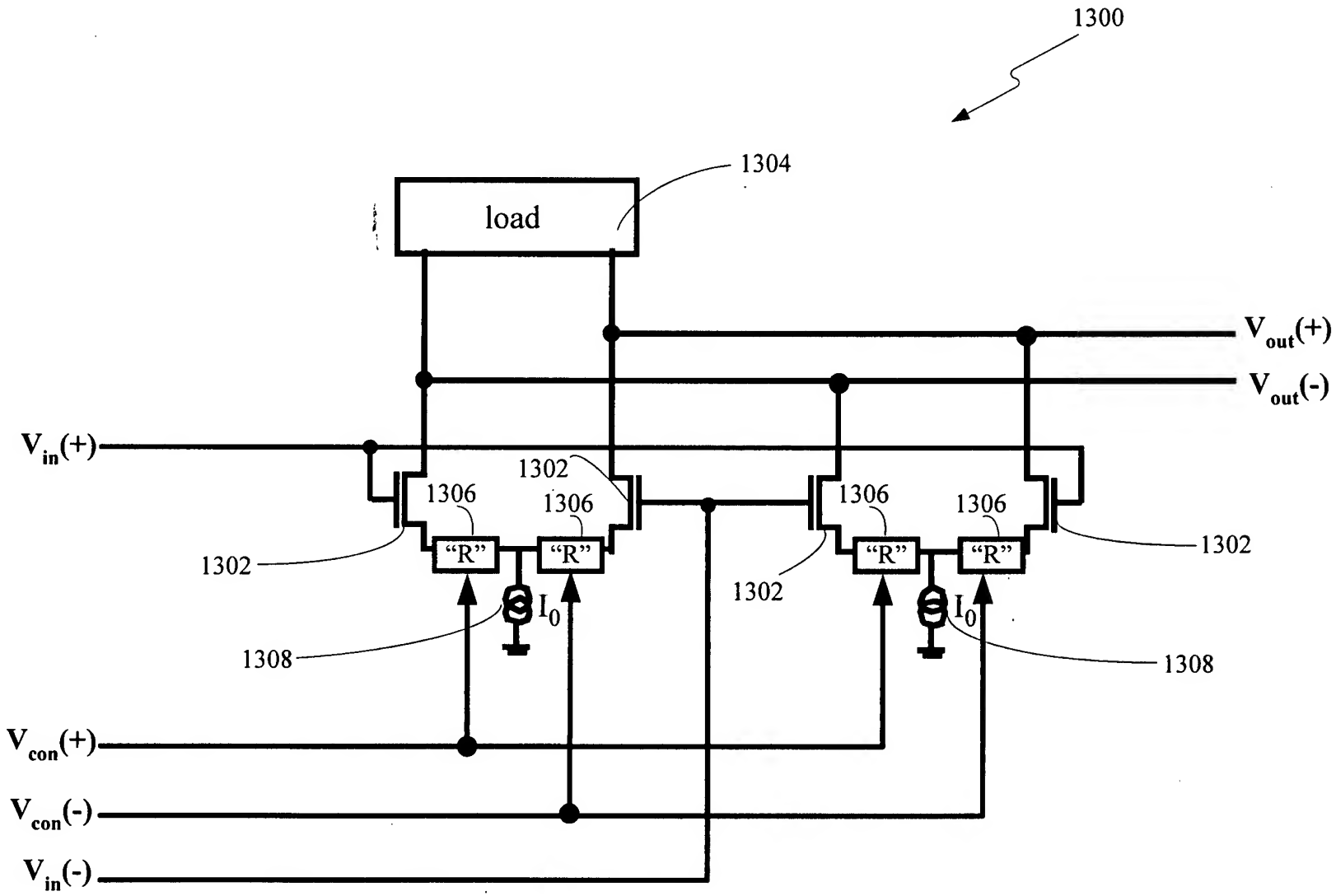
1300
1304
load
$V_{out}(+)$
$V_{out}(-)$
$V_{in}(+)$
1302
1306
1306
"R"
"R"
1302
1308
I_0
1306
1306
"R"
"R"
1302
1302
I_0
1308
$V_{con}(+)$
$V_{con}(-)$
$V_{in}(-)$

Figure 13

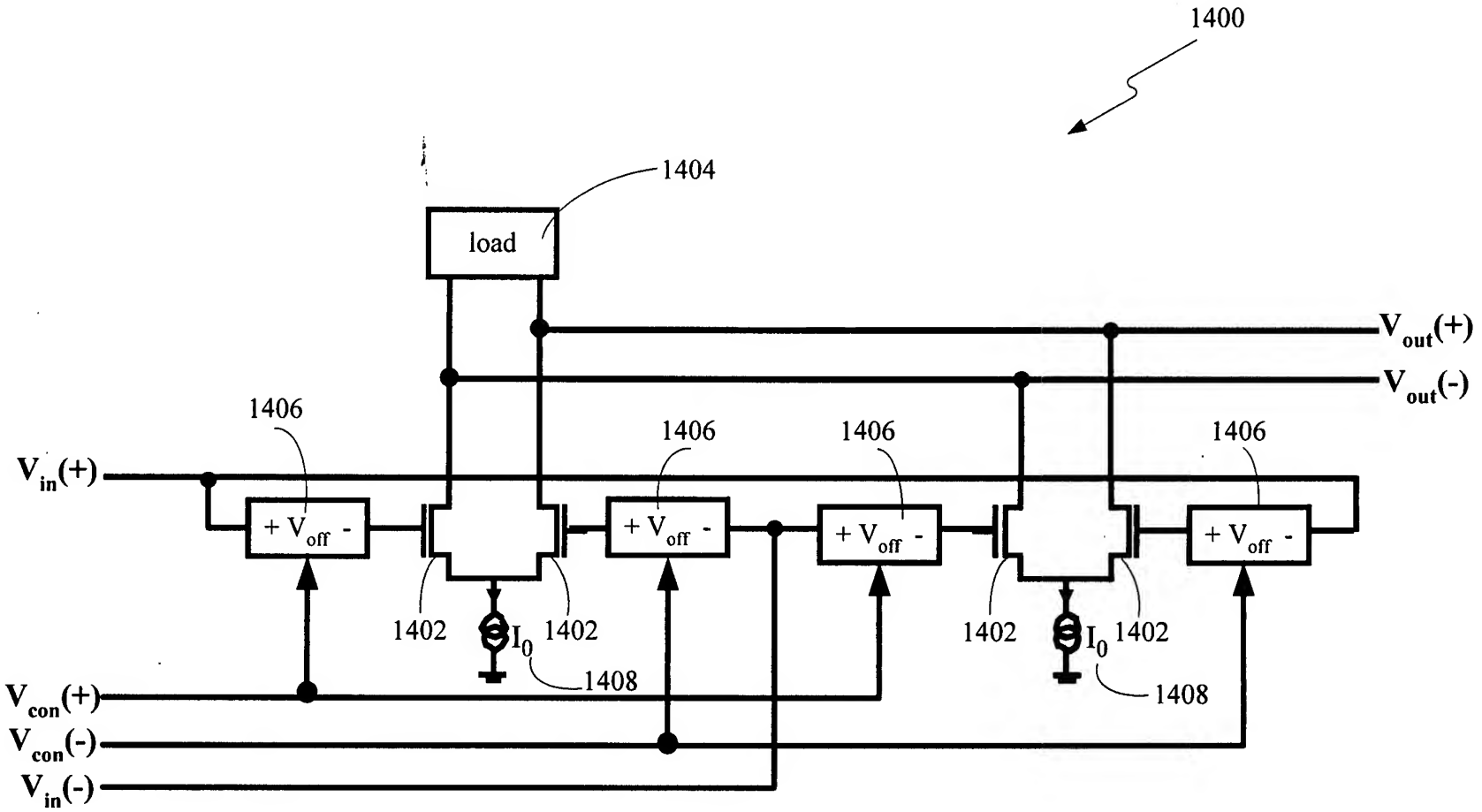
1400
1404
load
$V_{out}(+)$
$V_{out}(-)$
1406
1406
1406
1406
$V_{in}(+)$
+ V_{off} -
+ V_{off} -
+ V_{off} -
+ V_{off} -
1402
I_0
1402
1402
I_0
1402
1408
1408
$V_{con}(+)$
$V_{con}(-)$
$V_{in}(-)$

Figure 14A

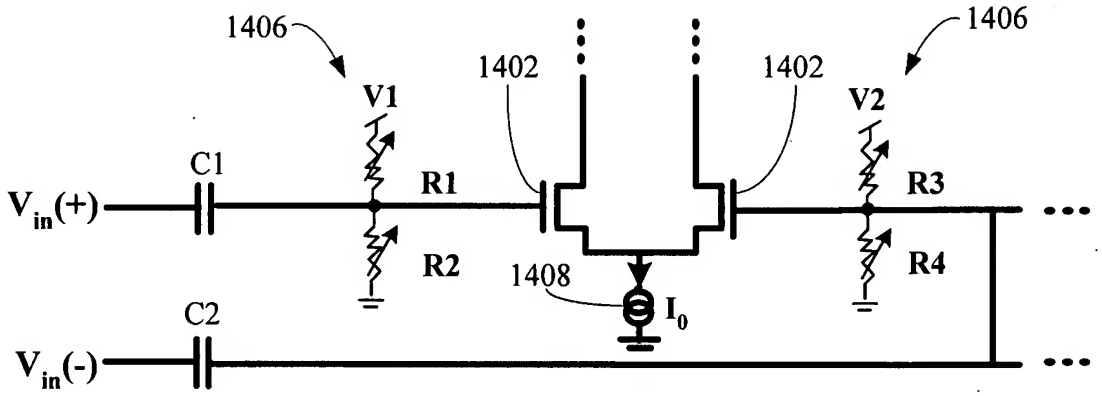

Figure 14B

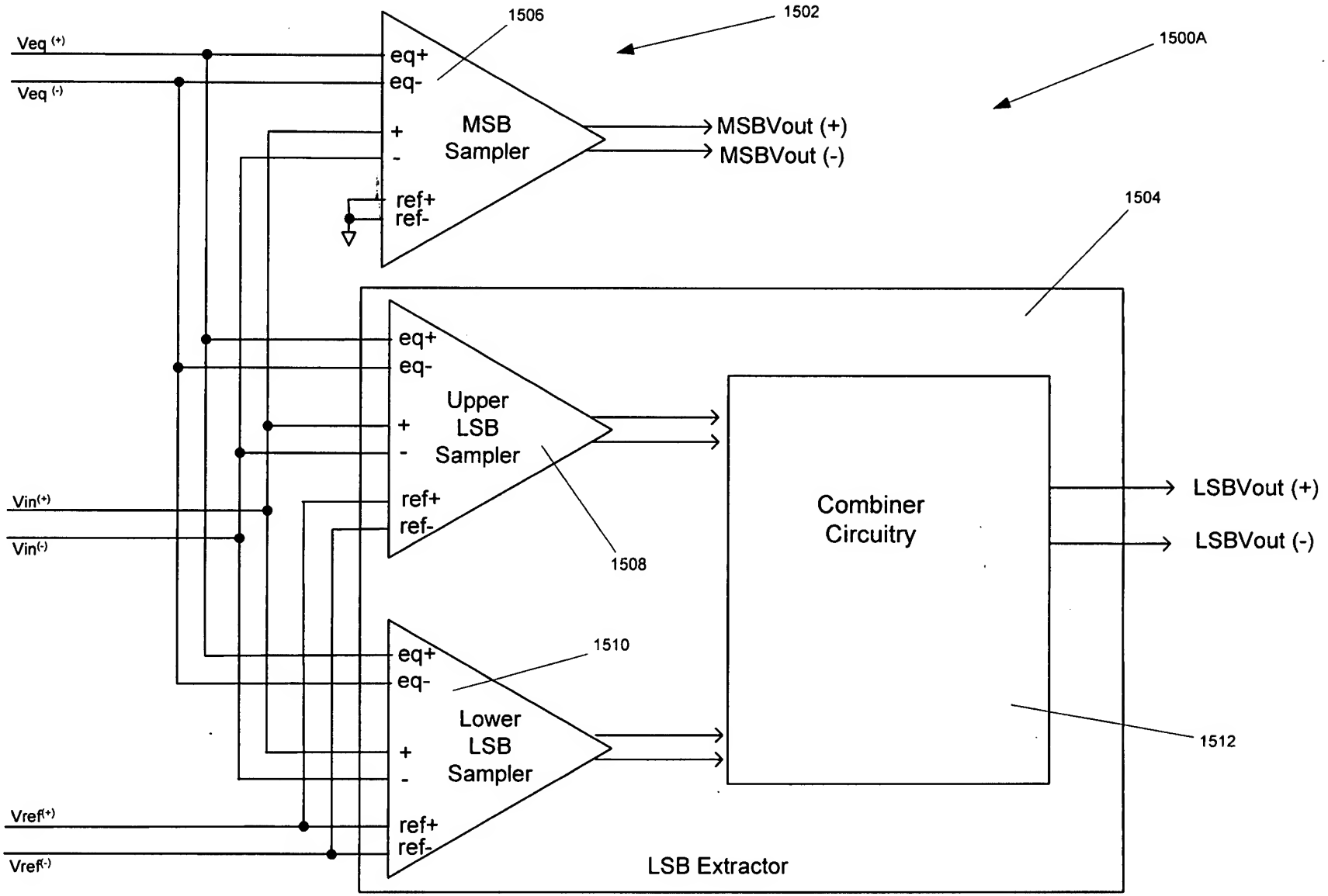
1506
1502
1500A
Veq (+)
Veq (-)
eq+
eq-
+
-
MSB
Sampler
MSBVout (+)
MSBVout (-)
ref+
ref-
1504
eq+
eq-
Upper
LSB
Sampler
+
-
ref+
ref-
1508
Vin(+)
Vin(-)
Combiner
Circuitry
LSBVout (+)
LSBVout (-)
1510
eq+
eq-
Lower
LSB
Sampler
+
-
ref+
ref-
1512
Vref(+)
Vref(-)
LSB Extractor

Figure 15A

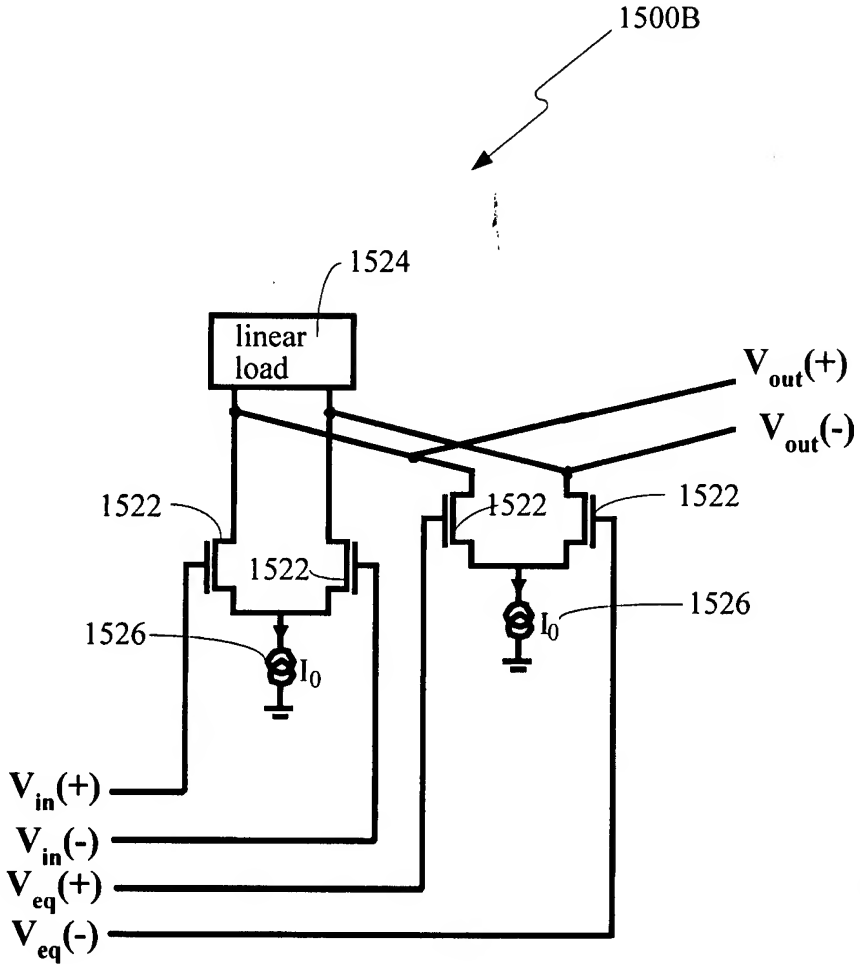

Figure 15B

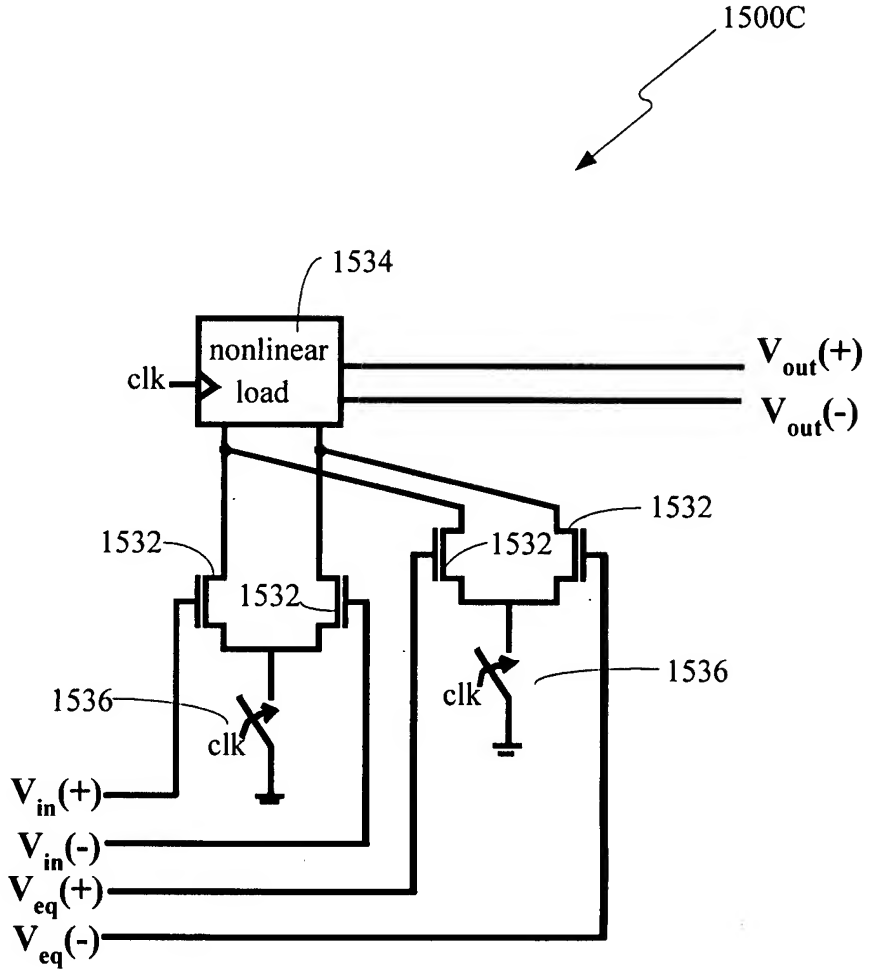

Figure 15C

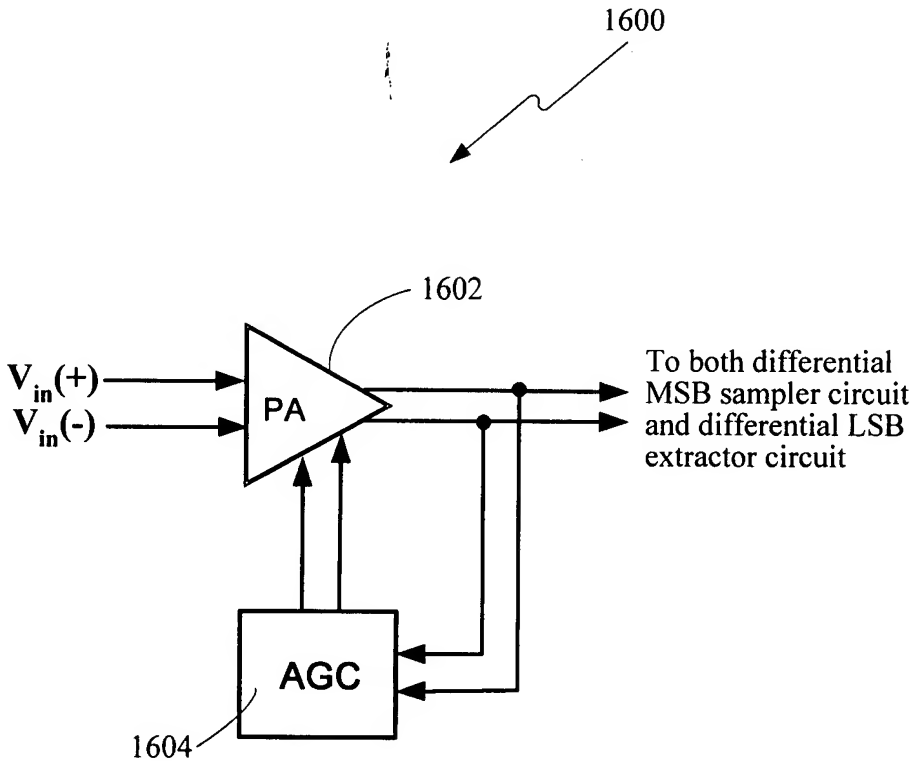

Figure 16A

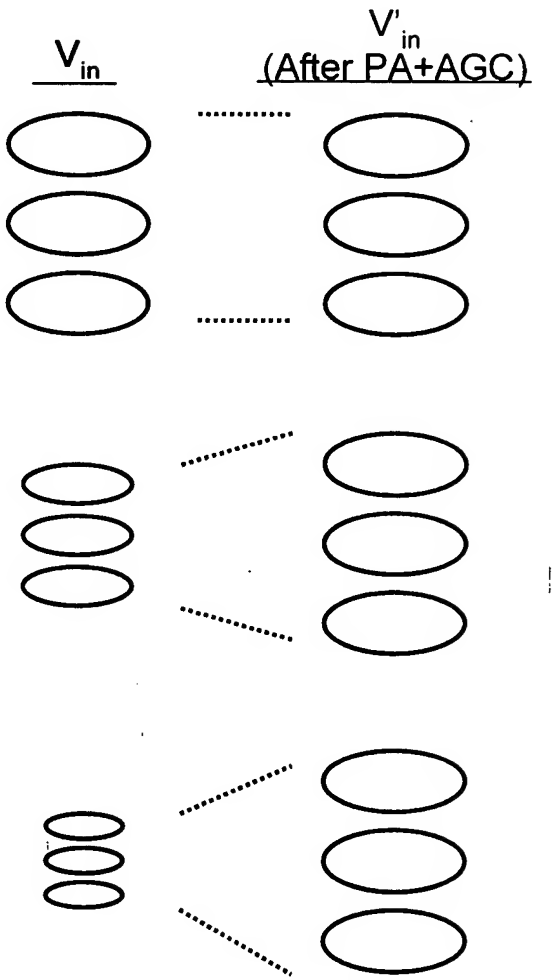

Figure 16B

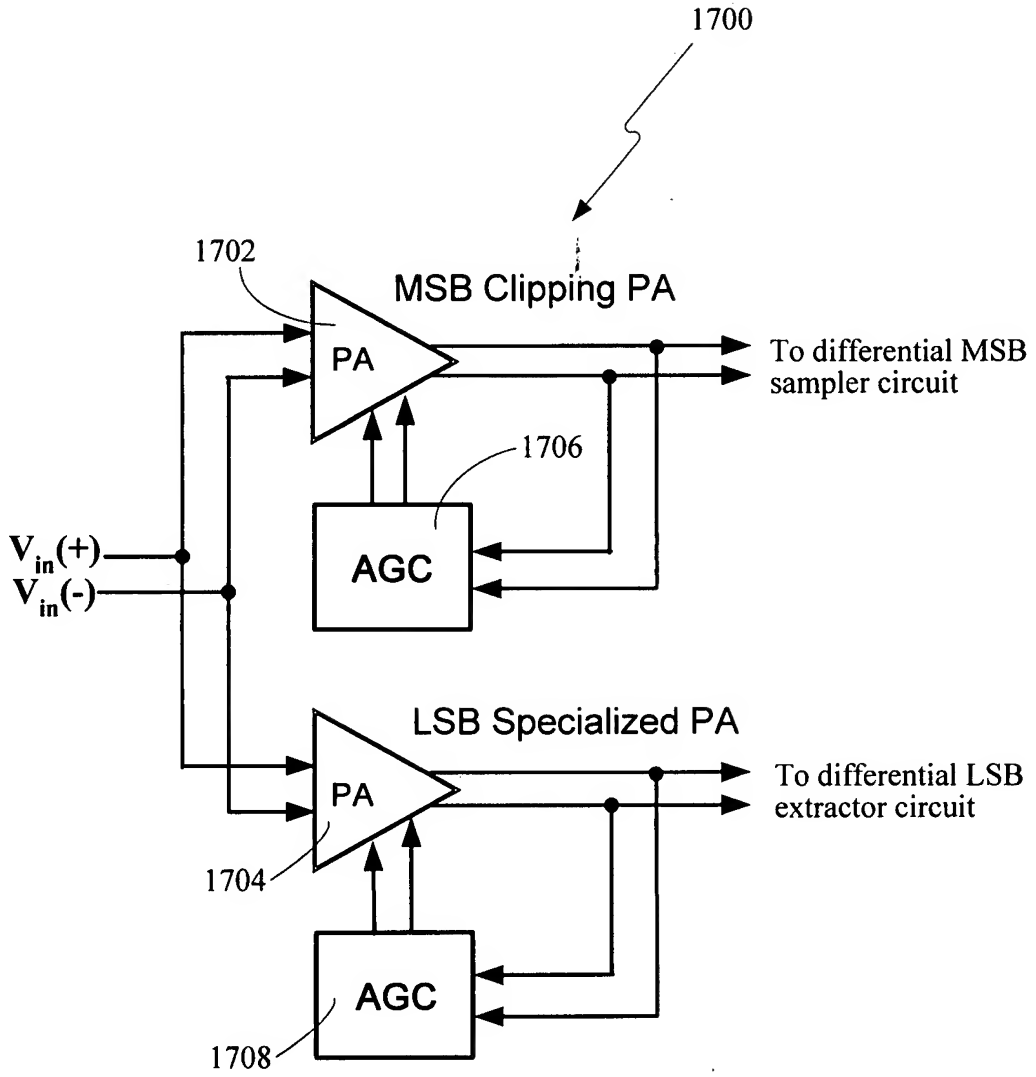

Figure 17A

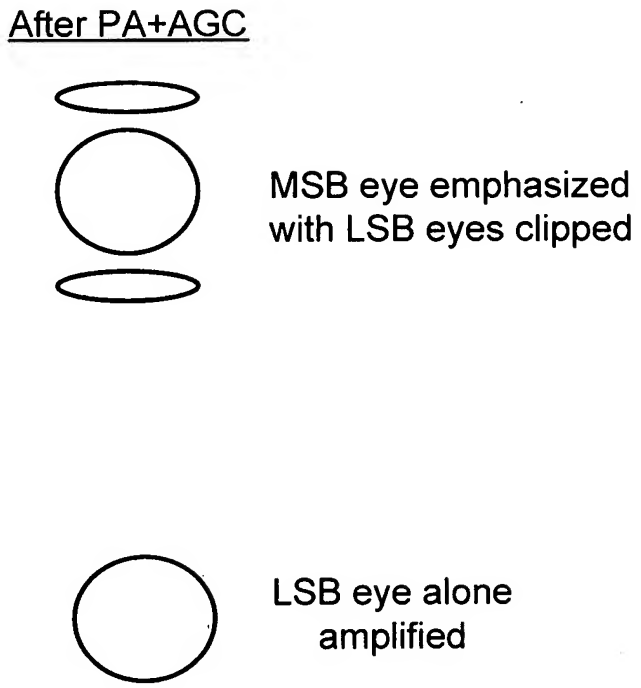

Figure 17B

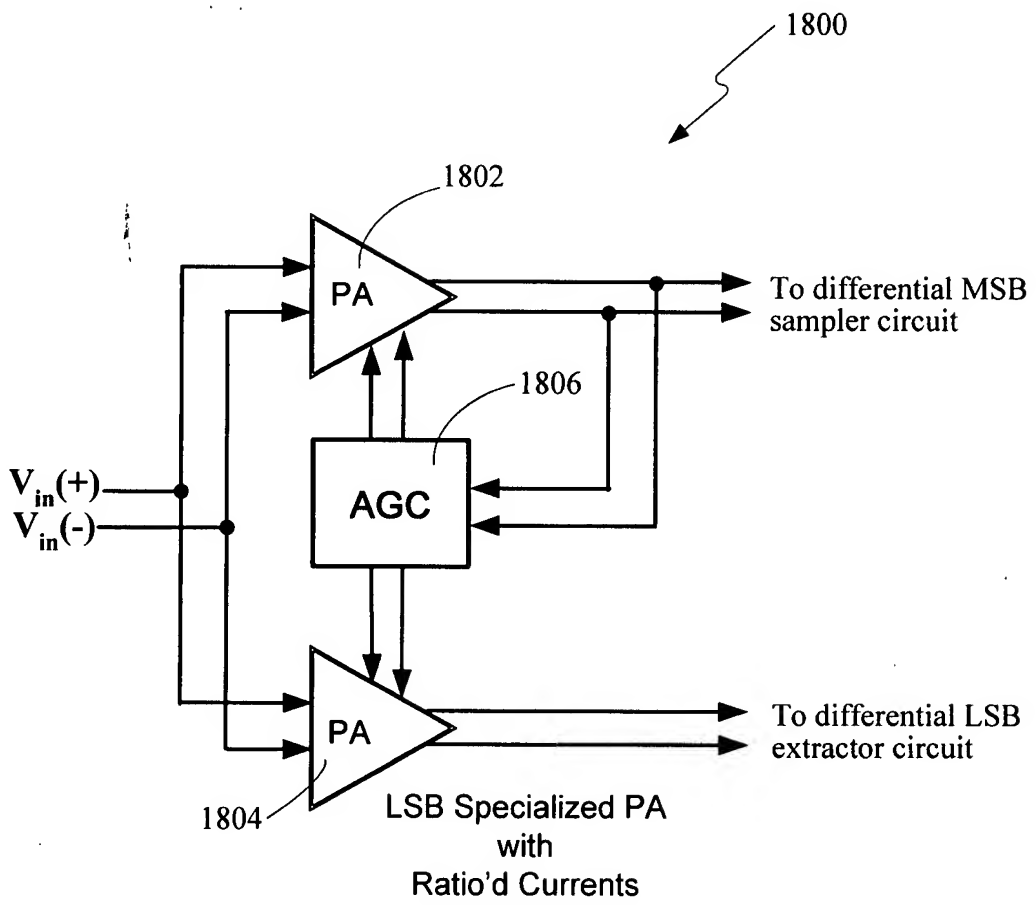
1800
1802
PA
To differential MSB
sampler circuit
1806
AGC
$V_{in}(+)$
$V_{in}(-)$
PA
To differential LSB
extractor circuit
1804
LSB Specialized PA
with
Ratio'd Currents

Figure 18

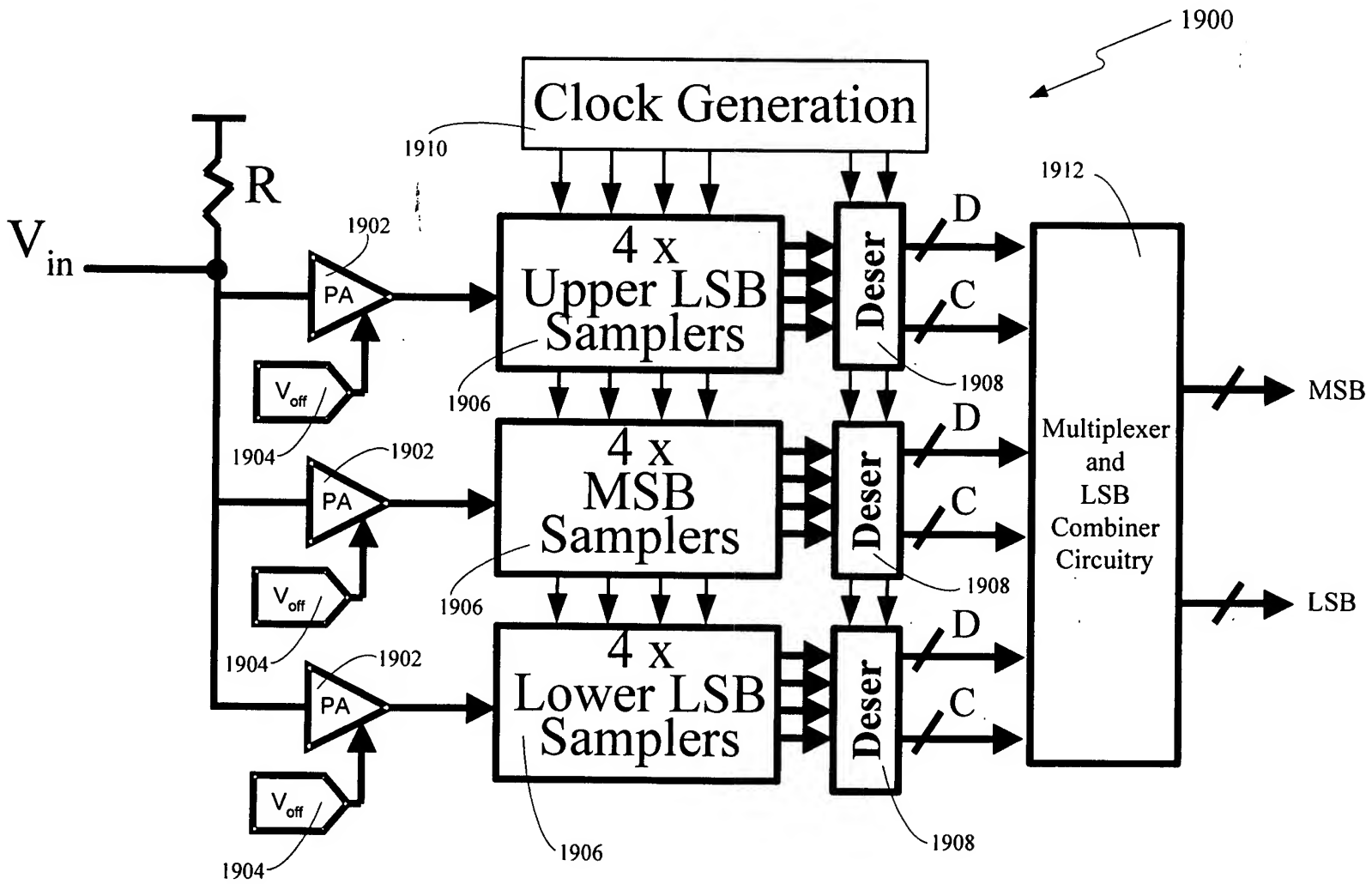
1900
Clock Generation
1910
R
V_{in}
1902
PA
V_{off}
1904
4 x
Upper LSB
Samplers
1906
Deser
D
C
1908
1912
4 x
MSB
Samplers
4 x
Lower LSB
Samplers
Multiplexer
and
LSB
Combiner
Circuitry
MSB
LSB

Figure 19

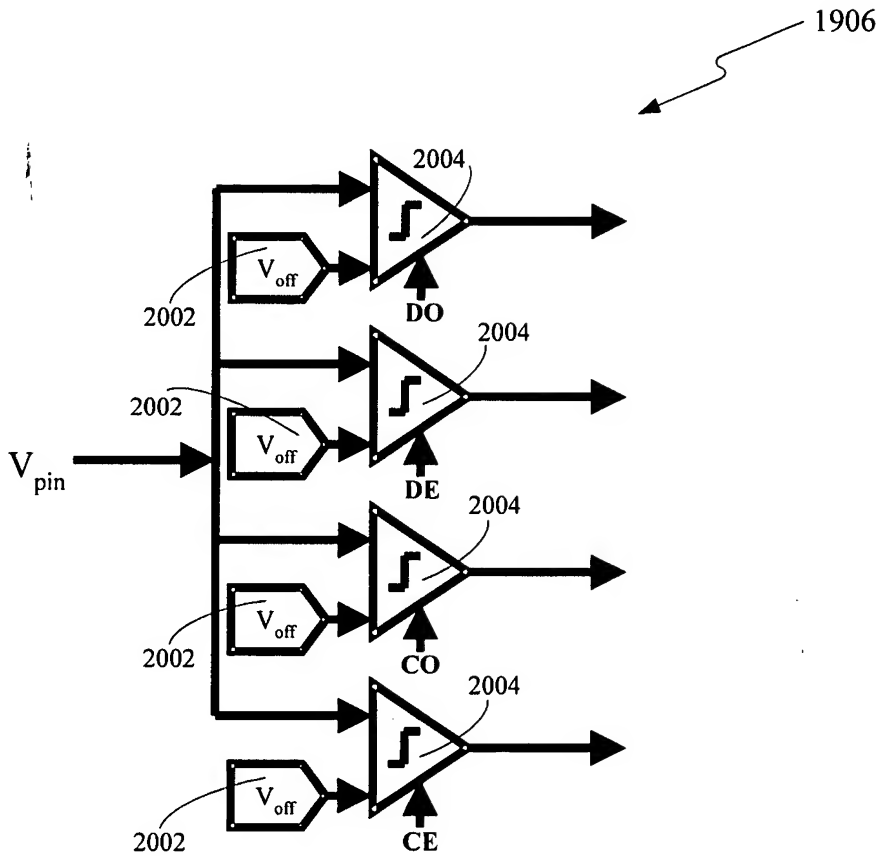
1906
2004
V_{off}
2002
DO
2004
2002
V_{off}
V_{pin}
DE
2004
V_{off}
2002
CO
2004
V_{off}
2002
CE

Figure 20

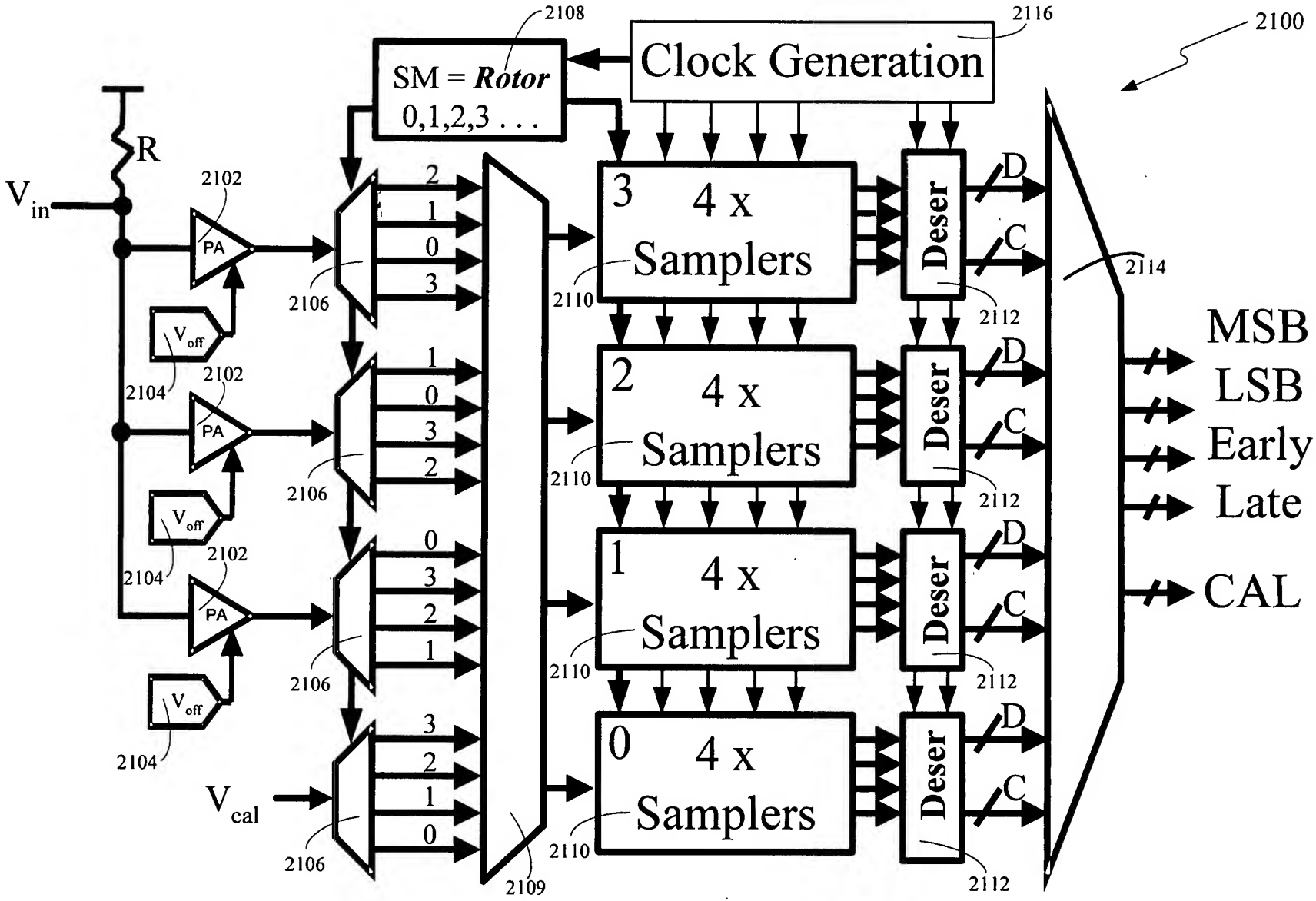
2100
2108
2116
SM = Rotor
0,1,2,3 . . .
Clock Generation
R
V_{in}
2102
PA
V_{off}
2104
2106
2110
3
2
1
0
4 x
Samplers
Deser
D
C
2112
2114
MSB
LSB
Early
Late
CAL
V_{cal}
2109

Figure 21

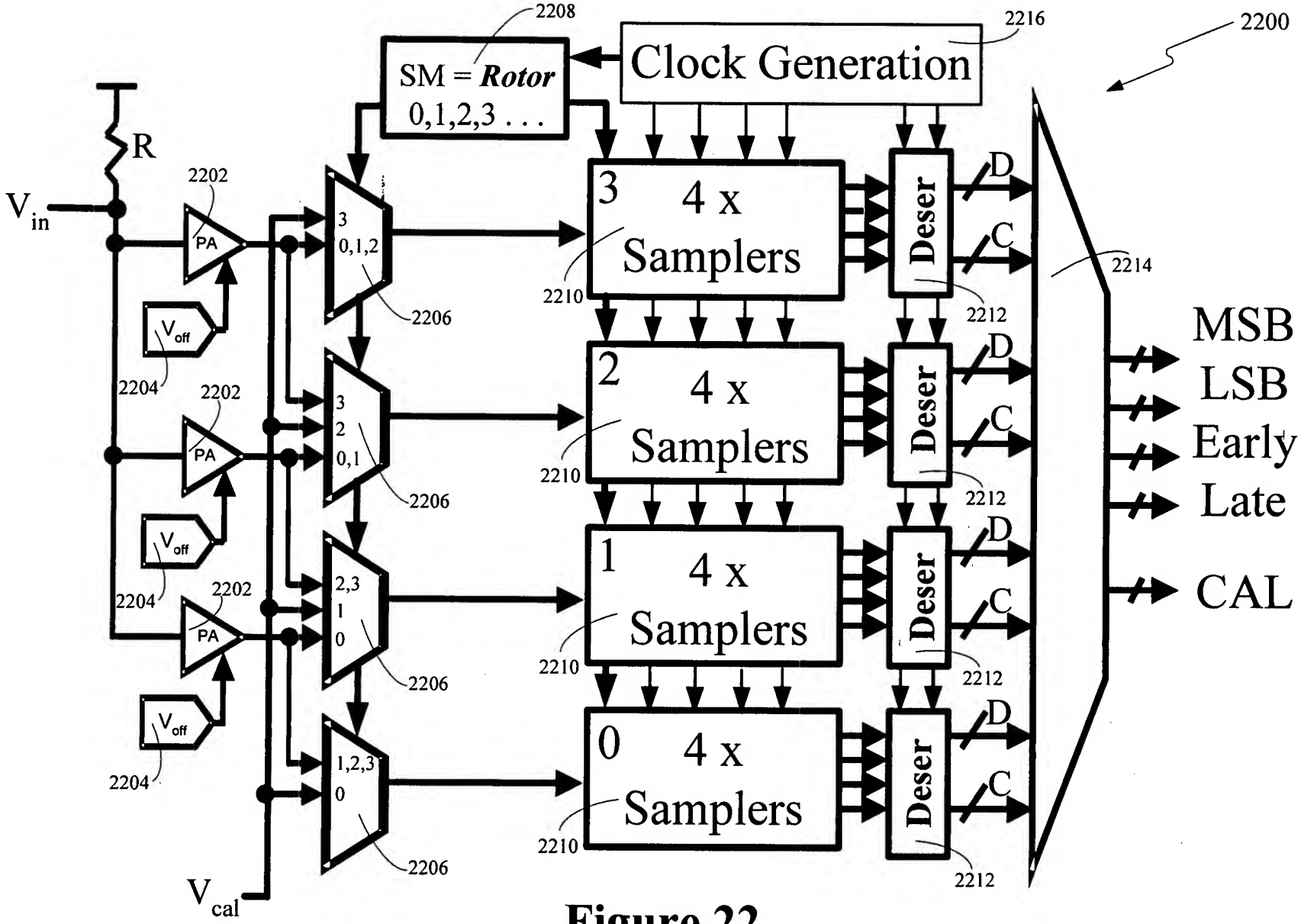
2208
SM = Rotor
0,1,2,3 . . .
2216
Clock Generation
2200
R
V_{in}
2202
PA
V_{off}
2204
3
0,1,2
2206
3
4 x
Samplers
2210
Deser
D
C
2212
2214
2
0,1
1
2,3
0
1,2,3
MSB
LSB
Early
Late
CAL
V_{cal}

Figure 22

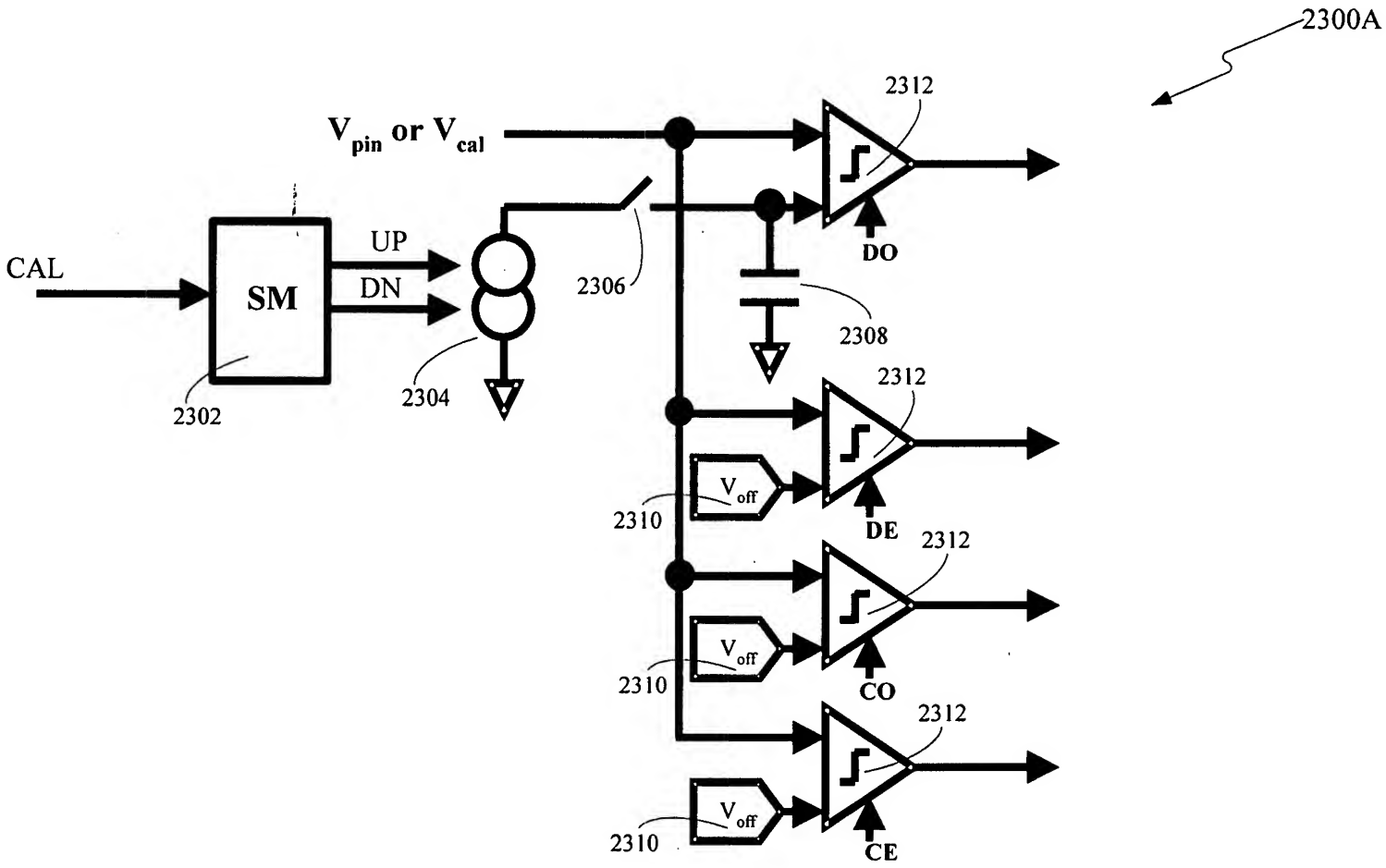
2300A
2312
V_{pin} or V_{cal}
CAL
SM
UP
DN
2302
2304
2306
DO
2308
2312
V_{off}
2310
DE
2312
V_{off}
2310
CO
2312
V_{off}
2310
CE

Figure 23A

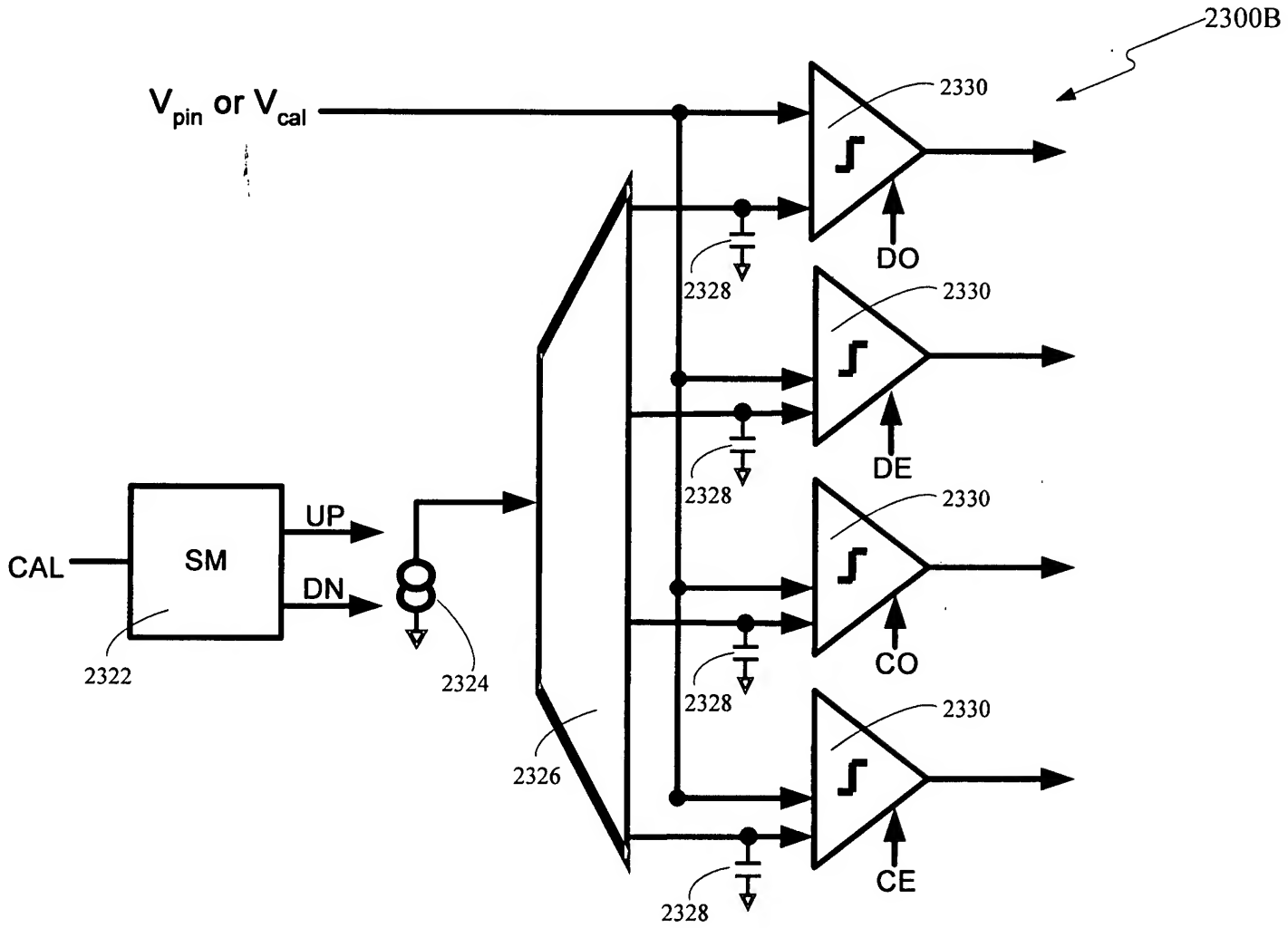
2300B
V_{pin} or V_{cal}
2330
DO
2328
2330
DE
2328
2330
CO
2328
2330
CE
2328
CAL
SM
UP
DN
2322
2324
2326

Figure 23B

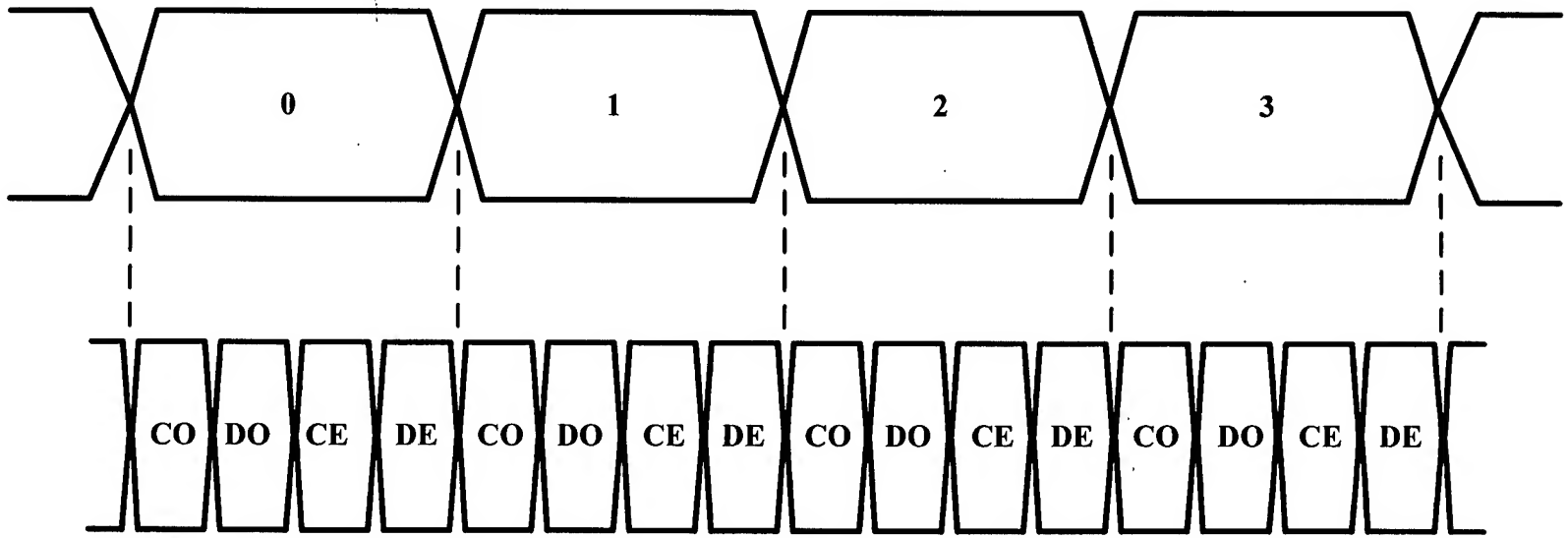

Figure 24